The Design and Simulation of 2.294dB Noise-Figure RF Wideband PHEMT LNA Employing 2-Stage Cascade with Single Feedback

Pramod K B & Praveen K B

Department of Electronics Engineering, Jain University, Bangalore, Karnataka, India
Department of Telecommunication, Dr. Ambedkar Institute of Technology, Bangalore, Karnataka, Inida
E-mail : pramod63putta@putta@gmail.com, prvn.guru@gmail.com

***Abstract* – This paper presents the design and simulation of 2-stage low noise amplifier(LNA) for the application of VHF and UHF range used for mobile satellite communications by using microstrip technology and focusing on development of low noise amplifier operating on the band of frequencies from 50M-1GHz by using Enhancement Mode Pseudomorphic HEMT ATF-53189 from Avago Technologies. The designed circuit uses lumped elements to implement the matching networks and purpose 2-stage is to achieve considerable gain. Input and output matching network is to produces 50Ω impedance for maximum power transfer. The target simulation are gain (S21) with >22 dB, noise figure (NF) with <4dB throughout the band from 50M -1GHz. A 2- stage LNA has successfully designed and simulated with 22 dB forward gain, 2.294 dB noise figure by using Advance Wireless Revolution (AWR) Microwave office tool.**

Keywords – Advance Wireless Revolution, Low Noise Amplifier, Radio Frequency, Noise Figure, And Pseudomorphic High Electron Mobility Transistor

I. INTRODUCTION

The low noise amplifiers (LNA) is a key electronic device used to filter out the noise of input signals received at the front end of communication systems, by possibly very weak signals from the antenna for the reduction of external as well as internal noise of the circuit [1]. Low noise amplifier is used in a wide variety of applications in RF communication systems such as wireless computer networks, mobile phones, and satellite receiver. Its plays as the significant components in the receiving end of the any communication system and its performance measured based on the Noise Figure, Gain in a Dynamic range, and stability.

II. SPECIFICATION, RESEARCH AND COLLECTED DATA

The five fundamental parameters of the LNA are: Gain, Bandwidth, Noise Figure, Linearity, and Power Consumption. The goal of designer is to minimize noise figure by considerable high gain with moderate linearity and establishing good impedance matching to other transceiver blocks. The additional constraint of low power consumption is imposed in portable systems.

In this reference [2] C. J. Jeong, they have presented an ultra-low power CG LNA design for WSN application. By adopting current-reused self biasing and forward body biasing techniques, the ultra-low power LNA design can be achieved. The measurement results show 1 to 3 GHz wide input matching, a 13.9 dB peak gain, 5.14 dB NF and -9.8dBm IIP3 while consuming 140 uA from a 1.5 V supply.

Reference of [3] Ping Zhou, in their paper they have presented a W-band low noise amplifier module using MMIC LNA chip has been successfully developed. The achieved linear gain of the LNA module is more than 23 dB in the frequency range from 92 to 94 GHz, and the noise figure at room temperature is about 5 dB.

Reference of [4] Tan Thiam Loong, in their paper a wideband LNA is demonstrated gain of 13.7 dB, 13.5 dB to 12.6 dB and 2.98 dB to 3.12 dB for the operating frequencies 1.575 GHz, 2.11 GHz to 2.17 GHz and 2.4 GHz to 2.48 GHz, respectively. The minimum gain achieved in this large of frequencies is of 10.3 dB while the maximum NF is 3.12 dB. Total power consumption is 14.4 mW.

III. LOW NOISE AMPLIFIER TRANSISTOR SELECTION

Selection of the transistor is the crucial stage in LNA design which is based on the data Maximum Available Gain (MAG), minimum intrinsic noise figure (NFmin) and frequency of the transistor. So after adding the matching and biasing sections, we cannot achieve gain more than MAG and Noise figure less than NFmin**.** To achieve a gain over 20 dB, a 2-stage LNA is designed, because the noise figure of the next stages is reduced by a factor equal to the total gain till that stage. It is observed that Transistor ATF53189 has the Noise Figure of 0.85 dB at bias point of 4V, IDS=135 mA 2 GHz and associated Gain of 17.5dB.

IV. STABILITY ENHANCEMENT CIRCUIT

When embarking on any amplifier design it is very important to check on the stability of the device chosen, otherwise the amplifier may well turn into an oscillator. The main way of determining the stability of a device is to calculate the Rollett's stability factor (K). Usually all the transistor available in market are unconditionally unstable and the necessary and sufficient conditions for unconditional stability are: K>1 and B1>0.

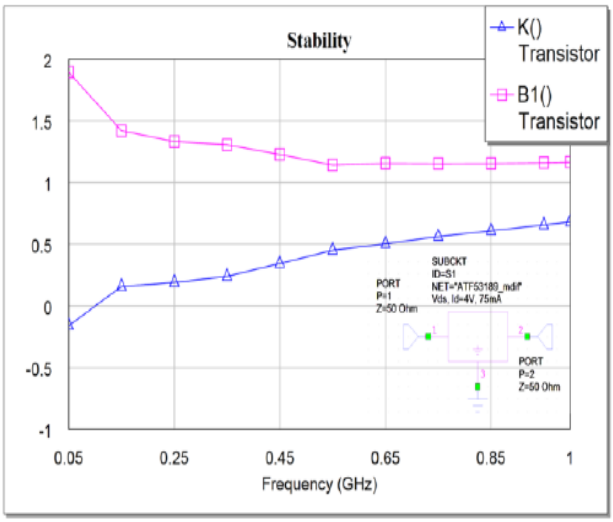

Fig. 1. Stability check of the bare transistor

K is the stability factor for a two port, defined as:

$$k = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}\cdot S_{21}|} > 1 \quad (1)$$

B1 is the supplemental stability factor for a two port, defined as:

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \quad (2)$$

where

Δ = S11S22 - S12S21

A transistor are stabilized by adding small series resistors or large shunt resistors to its input or/and output.

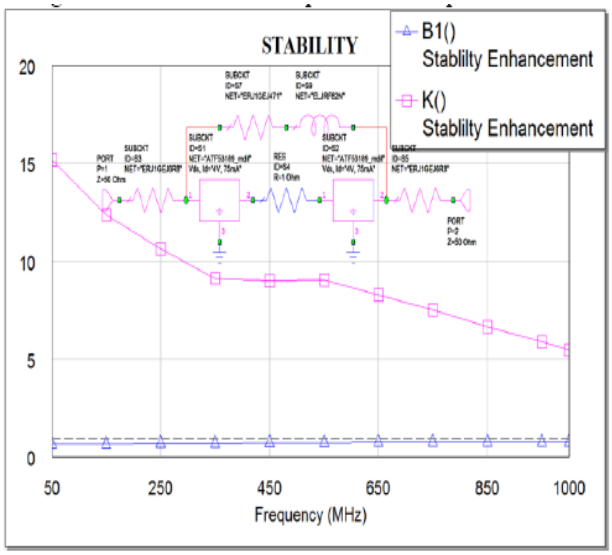

Fig. 2. Stability enhanced circuit with result

Now this circuit has satisfied conditions K > 1 and |Δ| < 1 B1 >0 becomes unconditionally stable to calculate the Maximum available gain (MAG):-

$$G_{MAX} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2-1}\right) \quad (3)$$

Where K is on the limit of unity the above equation reduces down to:-

$$G_{MAX} = \frac{|S_{21}|}{|S_{12}|} \quad (4)$$

V. NOISE FIGURE

Noise figure (NF) is a measure of degradation of the signal-to-noise ratio (SNR), caused by components in a radio frequency (RF) signal chain.

The noise figure is defined as:

$$NF = 10\log\frac{SNRin}{SNRout} \text{ in dB} \quad (5)$$

SNRin and SNRout are Signal to Noise ratio of the circuit or system at input and output

correspondingly.There are three key parameters that are needed for the noise figure analysis of an LNA with frequency , biasing condition are NFmin, Equivalent noise resistance Rn, and Optimum reflection coefficient Γopt

a. The Friis formula for noise factor

Friis's formula for total noise factor of a cascade of stages is given as

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \quad (6)$$

Where F_n and G_n are the noise factor and available power gain, respectively, of the n-th stage.

$$F_{receiver} = F_{LNA} + \frac{(F_{rest} - 1)}{G_{LNA}} \quad (7)$$

Where F_{rest} is the overall noise factor of the subsequent stages. According to the equation, $F_{receiver}$ the overall noise figure is dominated by the noise figure of the FLNA and GLNA the gain is sufficiently high.

b. The Friis formula for noise temperature

Friis's formula can be equivalently expressed in terms of noise temperature:

$$T_{total} = T_1 + \frac{T_2}{G_1} + \frac{T_3}{G_1 G_2} + \cdots \quad (8)$$

VI. INPUT MATCHING CIRCUIT

The matching for lowest possible noise figure over a band of frequencies requires that particular source impedance be presented to the input of the transistor. The noise optimizing source impedance is called as *Gopt*, and is obtained from the manufacturer's data sheet.

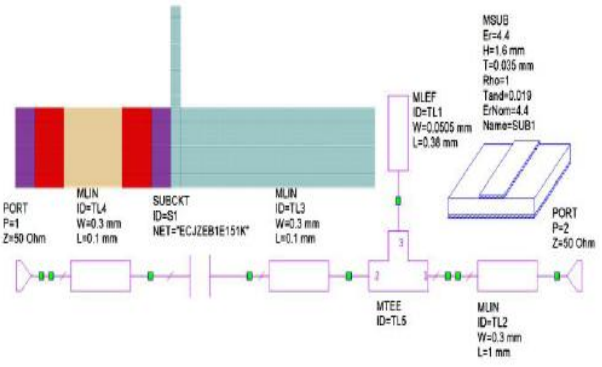

Fig. 3. Input matching circuit schematic with layout.

The above circuit shows the input matching circuit and process of layout involves the interconnection of MLINS, Tees between the elements. The layout obtained for the input matching network schematic and layout is shown in figure 3.

VII. OUTPUT MATCHING CIRCUIT

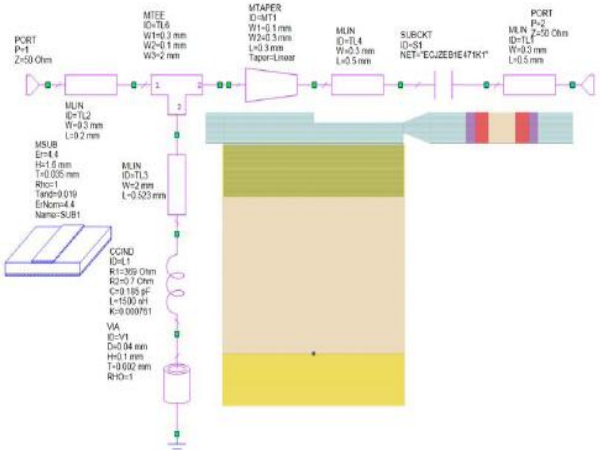

Fig. 4. Output matching circuit schematic with layout

The above figure 4 shows the schematic of output matching network followed by interconnecting the MLINS and MTEE for proper connection in layout.

In order to improve the gain and noise response of the final stage we need to provide the RL = ROUT* given by:

$$R_L = R_{OUT}^* = \left(S_{22} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_{opt}}{1 - S_{11} \cdot \Gamma_{opt}} \right)^* \quad (9)$$

VIII. MATCHING RESULTS

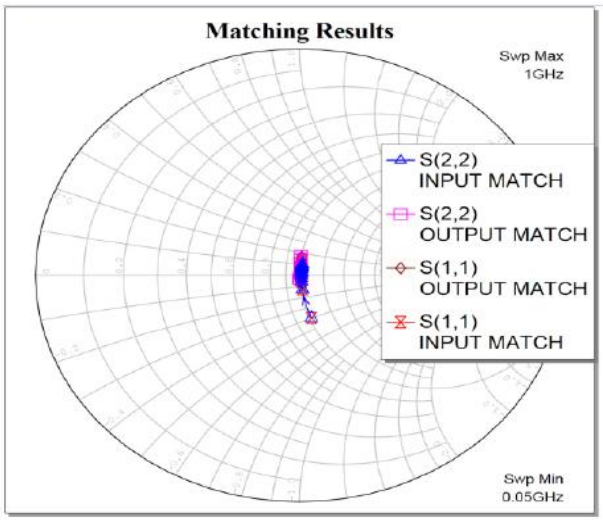

Fig. 5. Shows reflections at input and output in Matching circuits

Above Figure 5 graphs indicates matching circuits are good enough since all the points are very near at the center of smith chart (50Ω).

IX. IMPLEMENTATION OF THE DESIGN

The design implementation requires adding microstrip lines between the lumped elements and placing of micro strip Tee at the junction. The junction arm has to be extended using MLINS. The grounding must be done using via. The design is implemented on FR4 substrate with the relative permittivity €r=4.4 with a height of 1.6mm. The substrate thickness is chosen to be 0.035mm, Rho=1.

The below figure 6 shows the sub circuit of final schematic of an amplifier, the first sub circuit represents the input matching network.

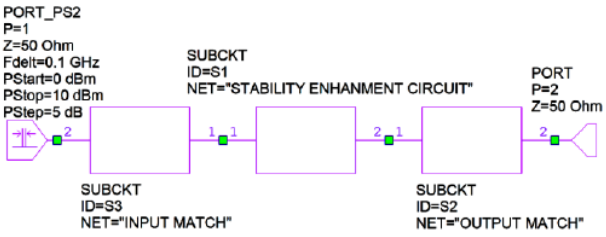

Fig. 6. Sub circuit of the complete schematic.

The grounding is done through vias which has the diameter of 0.254mm. The ratio of width and length should not be less than 0.254.To increase the gain of the amplifier second stage is designed. The second stage is designed in the same way as first using resistive loading.

X. BIAS NETWORKS

The proper bias or quiescent point for the application to maintain constant current over transistor parameter variations is required due to the process and temperature. The most critical device parameter commonly used in biasing is Idss, the saturated current at zero gate bias. The change of

I_D with V_G voltage is transconductance and is given by:

$$g_m = \frac{\Delta I_D}{\Delta V_G} \qquad (10)$$

XI. DRAIN AND GATE BIAS

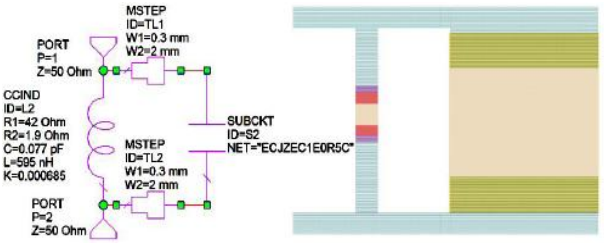

Fig. 7. shows drain bias circuit with layout

PHEMT Bias Conditions Both the gate and drain of a PHemt must meet bias conditions to Function properly. The drain voltage relative to the source (VDS) should be ≥ 2 V, while the gate voltage relative to the source (VGS) is used to set the current flow from the drain to the source (IDD).

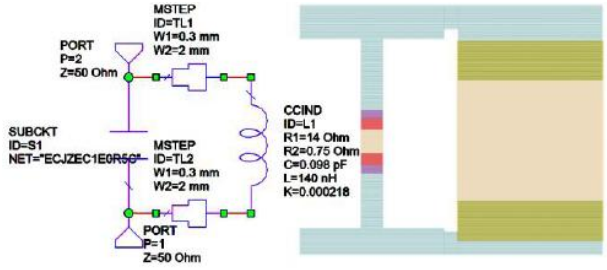

Fig. 8. Shows gate bias circuit with layout.

XII. BIASED STABILITY ENHANCEMENT CIRCUIT

In the former, a small resistance may be added in series with gate of the transistor. This technique is not used in LNA design because the resistance generates thermal noise, increasing the noise figure of the amplifier.

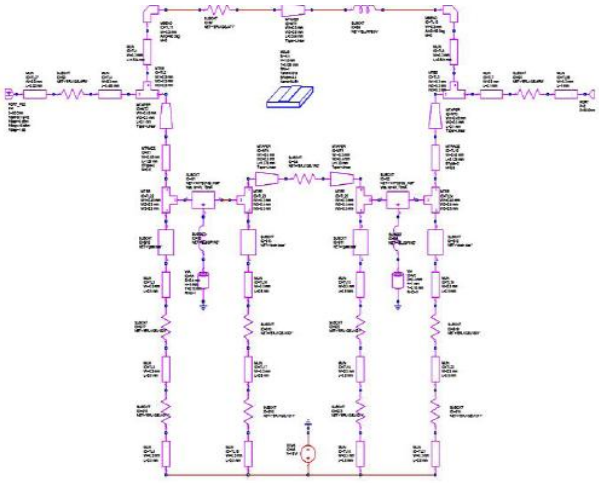

Fig. 9. Large Scale Analysis with biased circuit

Alternatively, an inductor may be added in series with the transistor gate. As an ideal inductor has zero

resistance, it generates no thermal noise. It improves stability by reducing the gain of the amplifier by a small factor.

XIII. VOLTAGE DROP CIRCUIT

Voltage drop is the reduction in voltage in the passive elements (not containing sources) of an electrical circuit. Voltage drops across conductors, contacts, connectors and source internal resistances are undesired as they reduce the supplied voltage (think: drain the battery) while voltage drops across loads and other electrical and electronic elements are useful and desired.

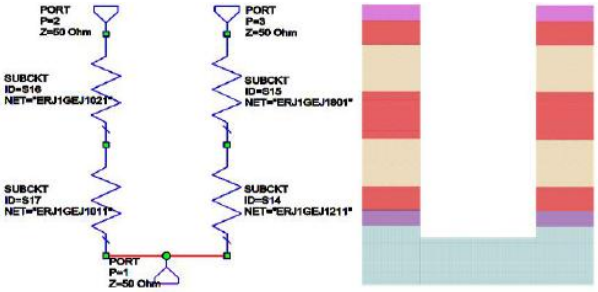

Fig. 10. Voltage Drop Circuit with layout.

Voltage drop circuit will helps to draw required voltage for both drain and gate from main supply (15V) without affecting any characteristics of the designed circuit.

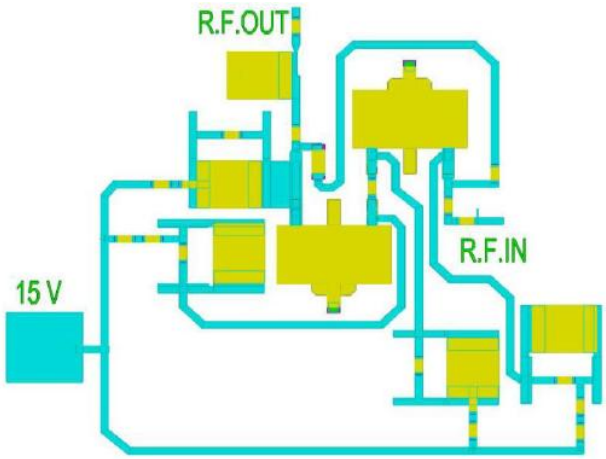

Fig. 11. complete layout of the Circuit

The Schematic View and the Layout View are two views of a single intelligent database that manages the connectivity between the circuit components. The layout of the schematic is shown figure 10.The 3x3 pads are used to provide supply to the gate and the drain of the transistor.

XIV. RESULTS ANALYSIS

The AWRDE features extensive post-processing capabilities, allowing the display of computed data known as "Measurements" on rectangular graphs, polar grids, Smith Charts, histograms, constellation graphs, tabular graphs, Antenna plots, and 3D graphs. The stability condition is satisfied which is shown in the figure 12 by Rollett's stability factor (K) > 1, MU1 > 1, MU2 > 1 and supplemental stability factor(B1) >0 for the entire frequency range.

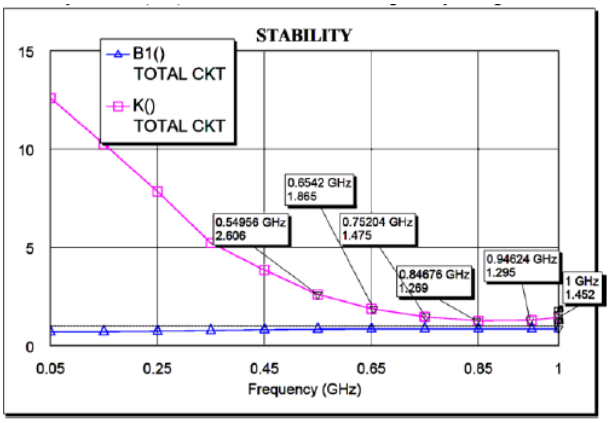

Fig. 12. Shows stability results

The maximum stable gain is the maximum gain that can be achieved by a potentially unstable device. Maximum stable gain is defined as the ratio of magnitude of S21 to the S12.The gain varies from 22dB to 23dB for the required frequency from 0.05GHz to 1 GHz. The graph plotted in the figure 13 shows the Maximum Stable Gain varying from 30dB TO 45dB.

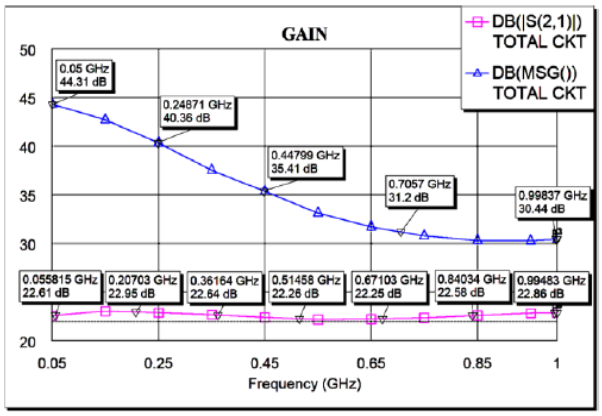

Fig. 13. Shows gain and maximum available gain

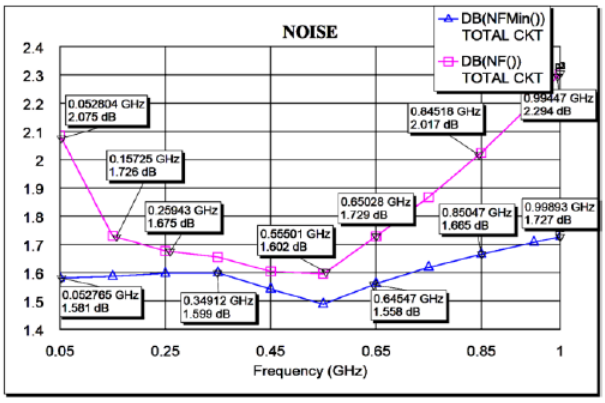

Fig. 14. shows noise figure and minimum noise figure

NFMin showed in the above graph shows that it is varying from 1.5dB to 1.7dB from the frequency 0.05GHz to 1GHz.Noise Figure varies from 1.604dB to 2.294dB.Required power output is 26dBm and in figure 12 shows the output power for 3 different input power throughout the band from 0.05GHz-1GHz and required output power 26dBm is achieved at input of 5dBm.

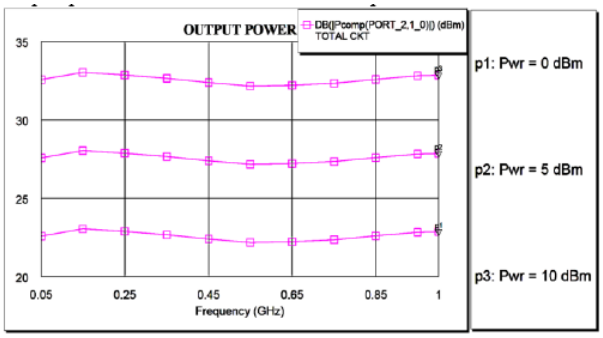

Fig. 15. Shows output power varies linearly with input power

XV. CONCLUSION

In this paper, a Wideband Low Noise Amplifier (LNA) circuit is designed successfully for frequency bandwidth of 950MHz (50MHz to 1GHz) with 22 dB gain and noise figure less than 2.294 dB throughout the frequency band using E-PHEMT **ATF-53189** by Avago technologies. Circuit simulation is done in **AWR Microwave Office 2010** with very good overall performance apart from the ultra low noise result.

References	Frequency (GHz)	Noise (dB)	Gain (dB)
[2]	2.2	5.14	13.9
[3]	92-94	5	23
[4]	1.575-2.48	3.2	13.7
This work	0.05-1	<2.29	22-23
This work	0.5	1.5	22.2

XVI. REFERENCES

[1] Design of a Low Noise Amplifier with GaAs MESFET at ku_Band Md. Rafiqul Islam, A.H.M. Zahirul Alam, Sheroz Khan, Arafat A. A Shabana Department of Electrical and Computer Engineering Faculty of Engineering International Islamic University Malaysia P.O. Box: 10, 50728 Kuala Lumpur, Malaysia E-mail: rafiq@iiu.edu.my

[2] A 1.5V, 140μA CMOS Ultra-Low Power Common-Gate LNA C. J. Jeong1, W. Qu2, Y. Sun1, D. Y. Yoon1, S. K. Han1, and S. G. Lee1 1Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon, 305-701, Korea, 2Silicon Works Company Ltd., Daejeon 305-380, Korea

[3] Design of A W-Band Low Noise Ampliifier Module With MMIC Ping Zhou, Pei Zhheng, Weihuua Yu, Houjuun Sun School of Infoormation and Electronics, BBeijing Institutte of Technoloogy, Beijing, 100081, Chinna E-mail: zhouping315@bit.edu.cn

[4] 1.575GHz to 2.48 GHz Multi-standard Low Noise Amplifier using 0.18-μm CMOS with On-Chip Matching Tan Thiam Loong#1, Awatif Hashim#2, Mohd Tafir Mustaffa#3, Norlaili Mohd. Noh#4 #School of Electrical & Electronic Engineering, USM, Engineering Campus, Nibong Tebal, 14300, Penang, Malaysia.

[5] Applied Wave Research, Microwave Office 9.04 Online Reference Manual.

[6] Ravinder Kumar1, Munish Kumar2, and Viranjay M, "Srivastava1DESIGN AND NOISE OPTIMIZATION OF RF LOW NOISE AMPLIFIER FOR IEEE STANDARD 802.11A WLAN" Department of Electronics and Communication Engineering, Jaypee University of Information Technology, Solan-173234, India.

[7] Viranjay M. Srivastava, K. S. Yadav, and G. Singh, "Analysis of double gate CMOS for double-pole four-throw RF switch design at 45-nm technology," J. of Computational Electronics, vol. 10, no. 1-2, pp. 229-240, June 2011.

❑❑❑