

DESIGN OF SPACE DATA LINK SUBLAYER OF TELECOMMAND DECODER USING CCSDS PROTOCOL

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Abstract- This paper deals with the design of Space Data Link layer of a Telecommand Decoder using CCSDS protocol. Telecommand Decoder is a part of Telecommand subsystem which receives uplinked data/commands and distributes it to all subsystems. All commands received will be validated and thereafter depending on the address, commands will be delivered to their respective destinations. Space Data Link sublayer was designed to meet the requirements of space missions for efficient transfer of space application data or commands to control the Spacecraft. Space Data Link modules are designed using CCSDS protocol and VHDL code for the same. Simulation is performed using modelsim.

Index Terms- CCSDS – Consultative Committee for Space Data Systems, CRC – Cyclic Redundancy Check , FARM – Frame Acceptance And Reception Logic, TC – Telecommand.

I. INTRODUCTION

Satellite communication is a complex process. Sending data commands or receiving data commands from ground station to spacecraft or vice versa is complex. Organizations like CCSDS have set some standards to simplify the communication system construction. The Consultative Committee for Space Data Systems (CCSDS) was formed in 1982 by the major space agencies of the world to provide a forum for discussion of common problems in the development and operation of space data systems. It is currently composed of ten member agencies, twenty-three observer agencies, and over 100 industrial associates. Since its establishment, it has been actively developing recommendations for data- and information-systems standards to reduce the cost to the various agencies of performing common data functions by eliminating unjustified project-unique design and development, and promote interoperability and cross support among cooperating space agencies to reduce operations costs by sharing facilities. CCSDS published several technical recommendations on data formats and transmission methods for telemetry and telecommand. The CCSDS telecommanding architecture defines a comprehensive set of layered, standardized command services which

are applicable to a very wide range of mission needs. This architecture will not only ease the transition towards the provision of more mission independent command services within each individual space agency, but also will promote technical harmony among all space agencies that can result in greater cross-support opportunities and services.

The OSI (open system interconnection) reference model is considered as the primary Architectural model generally applicable to any of a variety of technologies that provide for the exchange of information between real systems. Fig.1 depicts the relationship of the CCSDS Recommended Standard to OSI reference model .Two sublayers of the Data Link Layer are defined for CCSDS space link protocols. The TC Space Data Link Protocols corresponds to the Data Link Protocol Sublayer, and provides functions for transferring data using the protocol data unit called the Transfer Frame.

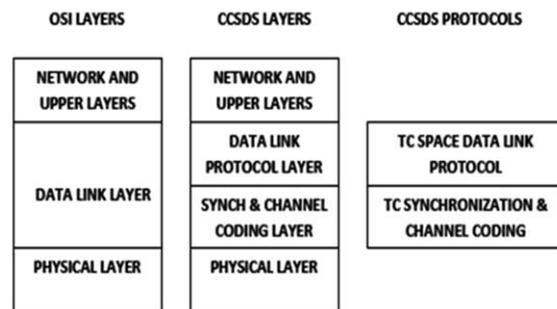


Fig. 1 Relationship with OSI layer

II. TELECOMMAND DECODER

Telecommand Decoder is a part of Telecommand subsystem which receives the uplinked commands and distributes it to all subsystems using secondary distribution. The Telecommand Decoder will have two separate serial input streams from receivers (through the Demodulator interface) comprising of serial data, clock and gated lock signals. All commands received will be validated and thereafter depending on the address delivered to their respective destinations using

secondary distribution. Hardware commands (on/off and data commands) will be delivered for secondary decoding through the Hardware Command Interface, while the Packet data/commands be delivered to the local processor through Peripheral Interface for further decoding and distribution. Packet data/command can also be delivered to the remote processor using the Remote Decoder Interface.

The Decoder can be configured to work in Clear-Mode or Secure-Mode. In Clear-Mode, the commands will be formatted using CCSDS format and uplinked. The Telecommand system will verify the commands for errors and its validity. The validated commands will be then distributed through the MAP Interfaces (i.e. Hardware Interface, Peripheral Interface or the Remote Decoder Interface). Generally this mode is used during the initial phase and Contingency periods.

In Secure-Mode the commands/data will be enclosed into a Security Protocol Frame, encrypted, CCSDS formatted and then uplinked. The received commands will be checked for errors, validated, decrypted and authenticated before being distributed through the MAP Interfaces. Any Clear-Mode command or a non-authentic Secure-Mode command received in the virtual channel which is in the Secure-Mode will be rejected. For security reasons both channels should be in Secure-Mode.

The decoder is divided logically into Coding and Synchronization Sublayer, Space Data Link Sublayer, Data Transfer Layer and other unit's viz. Time Keeping Unit, Memory Arbitration Unit, Configuration Unit and Decryptor Unit for supporting functions.

III. SPACE DATA LINK LAYER

The Space Data Link Protocols are protocols of the Data Link Layer of the OSI Basic Reference Model. They were designed by CCSDS to meet the requirements of space missions for efficient transfer of space application data of various types and characteristics on space links. Most of the present-day spacecraft use micro-processors for processing data (e.g., for compressing data, checking the status of subsystems, executing timelines, etc.). As a result, they need to send and receive various types of data (e.g., compressed images, housekeeping telemetry, event reports, commands, timelines, etc.) that have different Quality of Service (QoS), requirements in terms of data volume, data rate, latency, reliability, and so on. However, since the processing capability available onboard spacecraft is limited due to the physical constraints imposed by the fact that the

spacecraft are flying, the protocols must be simple enough to be implemented by small hardware and/or processors. The Space Data Link Protocols have the capability of transferring various kinds of data with different QoS requirements using relatively simple algorithms.

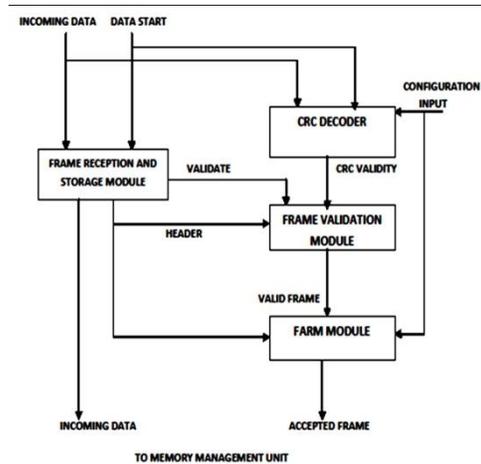


Fig. 2 Block diagram of Space Data Link Sublayer

Space data link layer provides the following four functions for transferring Transfer Frames over a space link:

- CRC decoder
- Frame reception and storage module
- Frame validation module
- Frame reception and acceptance mechanism (FARM) module.

The Frame Reception and Storage module perform the required functions to store the incoming frame in the memory. The remaining modules perform the validity checks for the frame.

The Frame Reception and Storage Module receives the information from the coding layer, extracts the header and stores the incoming data containing telecommand segments in the external memory.

The CRC Decoder performs the CRC validation on the incoming frame. Frame Validation Module checks the CRC and Static Field Checks (Spacecraft ID, Virtual Channel ID, Frame Length etc) when it receives a 'Validate' Signal from Frame Reception and Storage Logic. It shall generate a 'Valid Frame' Signal when the required checks are passed.

The FARM Module implements the FARM State Machine. It is activated by the 'Valid Frame' Signal. It generates the 'Frame Accepted' signal if the required

conditions are met as per FARM definition. The 'Frame Accepted' Signal is passed to the Memory Management unit which in turn invokes the Data Interface Module to read the data from the memory.

A. CRC decoder

Cyclic Redundancy Check is a form of integrity checksum. It is a powerful method for detecting errors in the received data by grouping the bytes of data into a block and calculating a Cyclic Redundancy Check (CRC). This is usually done by the data link protocol and calculated CRC is appended to the end of the data link layer frame. The CRC decoder is initialized to all ones, and the CRC is calculated over the entire Transfer Frame, including the Frame Error Control field, using the standard polynomial specified. The result of the CRC calculation is then verified to be zero.

Fig. 3 shows an arrangement for decoding using the shift register. When the Data Start and Data Window signal are asserted high, the Serial Data coming from the Coding Layer is shifted into the register. Whenever the value of the shift register becomes all zero, the CRC Validity Signal is set high indicating the reception of error free frame. All the other combinations indicate erroneous frame. The CRC Polynomial used is $x^{16} + x^{12} + x^5 + 1$ (CRC-CCITT).

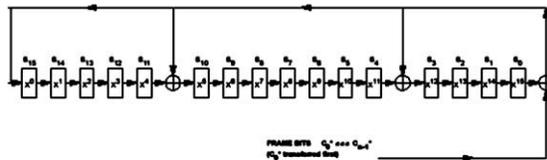


Fig. 3 Block diagram of CRC Decoder

B. Frame Reception module

The functional block diagram of the Frame Reception Logic is shown in Fig. 4 This module receives Serial Data, Clock and Data Start Signal from the Coding layer. It performs the function of reception and storage of the incoming frame. The Control command flag, Bypass Flag and Frame length fields in the received Frame Header is used to process the incoming data of a frame. When the Data Start signal is asserted, the Frame Octet Counter starts counting the number of octets received. The Frame Reception Control receives the serial data and routes it to three different registers according to the octet count and frame type. The sequence of operations is as follows.

- The first five octets are shifted into the frame header register. The header information shall be used to identify the type of Frame being received.
- If the header specifies the incoming frame to be of Type BC, the next one/three octets are shifted to the Control Command Register. This information shall be used by the FARM module to execute the commands.
- If the frame is of AD or BD type, the incoming octets are shifted into the Octet Register and then stored in memory.

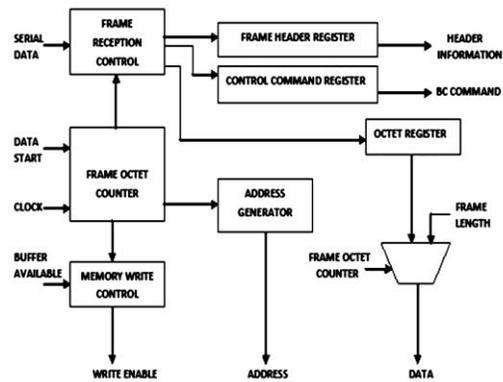


Fig. 4 Block diagram of Frame reception and storage module.

Memory Write Control generates the write enable signals for storing the incoming Frame Data Octets in the memory. The Write Enable signals are synchronized to the memory arbitration counter. Whenever the write cycle is being executed, a memory busy signal is asserted to indicate the other modules not to perform any memory transaction. When a BD Frame is being received, the write enable signal is always passed down. When an AD command is being received, the write enable signal is passed down when the buffer available signal is asserted. When receiving a BC frame, the write enable signals are arrested since no data is required to be written in memory. The address generator generates the appropriate address to store the incoming Frame Octets. The first two octets written into the memory specify the data length whose value is 7 octets (Header + CRC) less than the frame length. The following octets shall be filled by the data being received. When the number of octets received is equal to Frame Length as indicated in the Frame Header, the validate signal is generated. It shall be used by the Frame Validation Module for validating the current received frame.

C. Frame Validation module

Frame Validation Logic performs the clean and legal validation of the incoming frame. The functional block diagram of the module is given in Fig. 5. When it receives validate signal from the Frame Reception and Storage Logic, all the verification checks on header and data should have passed to get the final Frame Valid signal. The verification checks can be divided into two parts as described below.

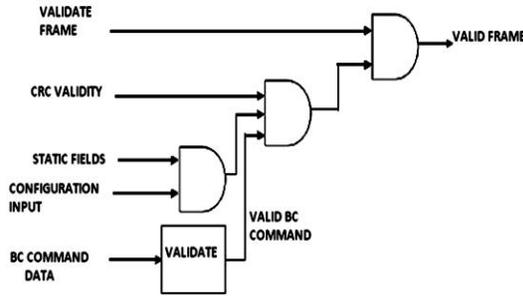


Fig. 5 Block diagram of Frame Validation module

a) Clean Transfer Frame Validation

Every candidate Transfer Frame received from the Coding Layer is verified to be clean by performing the following tasks.

- The number of octets received is verified to be greater than seven, i.e. at least two Code Blocks must have been received.
- The result of the CRC calculation is verified to be zero.

If the Transfer Frame passes all of the above controls, it is subjected to the Legal Transfer Frame Validation. If any of the controls fail, i.e. the frame is not clean; the candidate Transfer Frame is discarded and reported as being dirty.

b) Legal Transfer Frame Validation

Every clean Transfer Frame received from the Clean Transfer Frame Validation is verified to be legal by performing the following tasks.

- The static fields of the received Frame Header are verified to be identical to the value of the three Frame Header octets stored in external non-volatile memory, i.e. the Version Number, the Reserved field A, the Spacecraft Identifier, and the Virtual Channel identifier.
- The Transfer Frame type is verified to be an AD, a BC or a BD Frame. If the Transfer

Frame is of type BC, the Frame Data field is verified to contain either an 'Unlock' or a 'Set V(R) to V*(R)' FARM-1 Control Command.

- If the Transfer Frame is of type BC or BD, the Frame Sequence Number field is verified to be zero.

If any of the controls fail, i.e. the frame is not legal; the Transfer Frame is discarded and reported as being illegal. If the Transfer Frame passes all of the above controls it is transferred to the Frame Acceptance and Reporting mechanism.

D. FARM Module

The Frame Acceptance and Reporting Mechanism (FARM) is the core of the Telecommand Decoder. It is the satellite side part of the Communication operation procedure. The mechanism is responsible for the acceptance of frames and reports to the ground station about the current status of the frame data. Actions taken by the FARM depends on parts of the primary header of the Transfer frame. These parts are the Bypass Flag, the Control Command Flag and the Sequence Number of the Frame. The actions the FARM takes and the status of the FARM is reflected in the Communication Link Control Word (CLCW) which is periodically sent to the ground station.

FARM has 3 States namely

- Open
- Wait
- Lockout

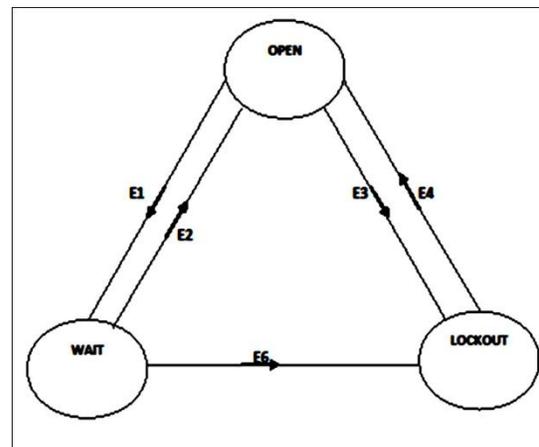


Fig. 6 FARM State transitions

In "Open" State, the protocol machine accepts in-sequence frames and passes them to the Higher Layer.

In “Wait” State, there is no buffer space available in which to place any further received Type-AD user data frames. The protocol machine enters the “Wait” State when it has received a Type-A TC data unit, but is unable to deliver it to the Higher Layer. It leaves the “Wait” State upon receipt of a buffer release signal from the Higher Layer.

In “Lockout” State the protocol machine receives a frame with sequence number N(S)outside the range expected if transmitter is operating correctly. It is a safe state in that no user data will be accepted or transferred to the Higher Layer when in the “Lockout” State (unless by pass is used). The protocol machine leaves the “Lockout” State upon receipt of an “Unlock” Control Command.

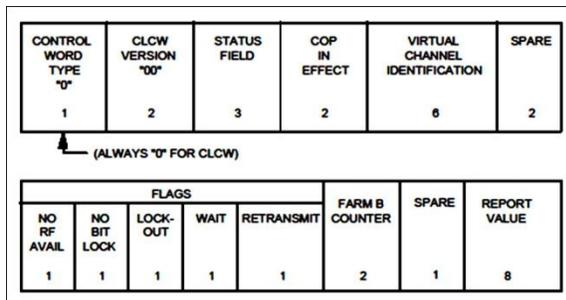


Fig. 7 Control Link Control Word Format

Bit 18 is set to value “1” to indicate LOCKOUT whenever a Type-A TC Frame is received on a particular Virtual Channel which violates certain frame acceptance checks. Once the FARM is in LOCKOUT, all subsequent Type-ATC Frames are rejected by that FARM until the condition is cleared. If the FARM is not in LOCKOUT, Bit 18 shall be set to value “0”.

When Bit 19 is set to value “1” (i.e., WAIT) for a particular Virtual Channel, all further Type-A TC Frames on that channel shall be rejected by the FARM until the condition is cleared by freeing the congestion, either automatically or by taking appropriate control action. When Bit 19 is set to value “0” (i.e., DON’T WAIT), normal Type-A commanding may proceed on that channel.

When Bit 20 is set to “0” it indicates that at the sending end one or more Type-A frames on a particular TC Virtual Channel have been rejected or found missing by the FARM and therefore retransmission is required. When Bit 20 is set to value “0”, this indicates that there is no outstanding Type-A frame rejections in the sequence received so far, and thus retransmissions are not required.

IV. SIMULATION RESULTS

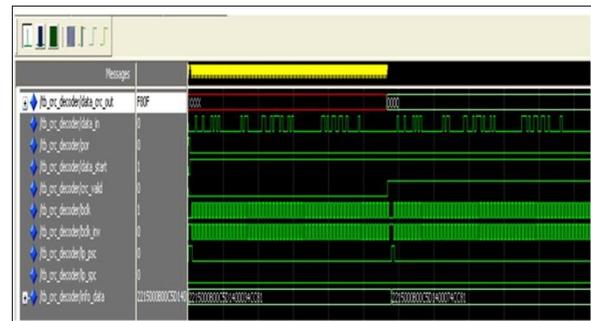


Fig. 8 CRC decoder output

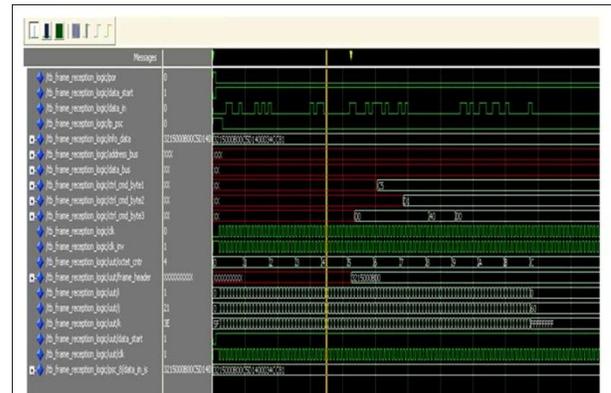


Fig. 9 Frame reception module output

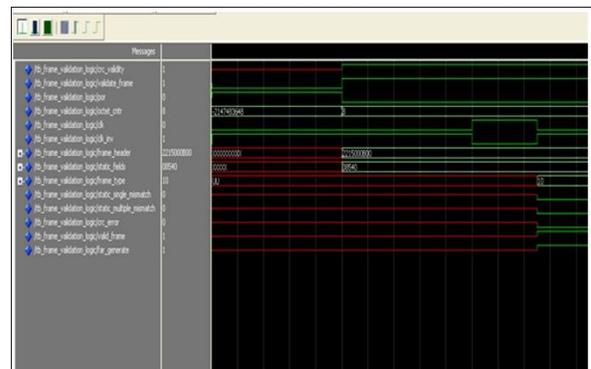


Fig. 10 Frame validation logic

V. CONCLUSION

In the present work the Space Data Link sublayer is designed using CCSDS protocol whose main function is to provide uplinked data to the data transfer layer and this design is mainly used in the telecommand core FPGA. The validate data can be designed and randomizer can be used for the CRC decoded data to improve bit transition density as an aid to bit synchronization.

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