OPTIMIZED CHARACTERIZATION METHOD OF IO'S OF INTEGRATED CIRCUITS

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***Abstract* - Today's Integrated Circuits have need to operate at very high IO speed to cater the ever increasing computation need, so characterizing these IO's in a quick efficient and accurate manner is needed for us. The paper involves studying Transmitter (T_x^{er}) and Receiver (R_x^{er}) blocks of memory interface of CPU and develop methods to characterized these IO's, suitable feedback to design is provided after analyzing the data and receiving with design. In this paper involves some analog analysis and design. Here it needs some software tool to implementation. This paper implements new method to increase the speed of the IO operations of the memory interface of CPU. This contain the usage of the NIDAQ6008 and analog design and the circuit design concepts and here it deals with the calculation of the Rterm, Pull-up, Pull-down resistors and Jitter and the de-embedding of the signal loss.**

***Index Terms*—Post Silicon Validation, Keithley Switch, Bipolar Constant Current Source, NI USB 6008, Python**

I. INTRODUCTION

System-level post-silicon validation is a function that is both resource intensive and time consuming. This being the last stage of IC development cycle, has considerable impact on time-to-market, quality and yield. The project is about increasing the efficiency of the process and improving the utilization of the equipment by automating switching, IO execution and data collection. In IO execution it is taking more time to complete, and also the cost of the setup is also reaches to high peaks. This allows validation-engineers to focus on speed of execution and cost of the setup, thus increasing the overall productivity of post-silicon validation process.

Post-silicon validation includes platform, IO execution, data collection & analysis and debugging the failures. And also the characterization of Transmitter and Receiver parts of the chip. The switching, data collection and IO execution is done over a large sample size with different process characteristics across different voltage and temperature conditions. Currently all of the above functions are being done manually, leading to huge time consumption and engineers' involvement in IO execution and data collection. This brings up need for automation of this process so that the speed is increased.

II. LITERATURE SURVEY

This project is about how advantage it is when compare to the older version. And this is increase the speed of the IO operation and save the money in order of thousand dollars and save time to IO operation. Previous they are supposed to use the serial data acquisition devices but now we are implemented parallel data acquisition methodology to reach our requirements.

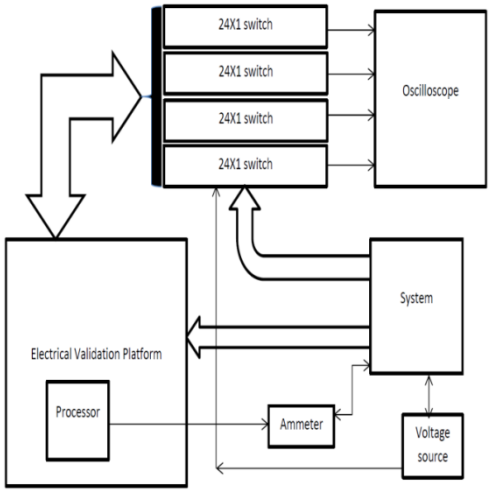

Figure 2.1: The block level representation of the present setup.

The above is the brief description of the individual parts of the old setup. It contain processor socket, it is used to place the chip in that socket and we can start the electrical validation process. Here it contains IO pin outs from that board, now we need to characterize the transmitter and receiver parts of the chip. Here the engineers main concentration about Transmitter characterization why because it include the more electrical parameters to analyze than Receiver part. And also the automation is less in the transmitter characterization method, it will take more time to complete the validation process it effects the time to

market and cost of the setup also more. To overcome these drawbacks designers are looking for the new design for the setup.

In above setup we are sending the pattern to that chip through the Keithley switch. It contain 3 stage relay switching network as shown below, it is a 24:1 mux type network here 24 IO pins are connected to one Keithley switch it will send the pattern to any one pin out of the 24 pins. But processor contains 4 channels, 72 DQ lanes and 17 CMD lanes per channel to cover all these lanes we need 4 Keithley switches.

It will be time consuming, and we have another way is that design 72:1 but it causes signal loss because of the more stages. And here we need to use Voltage source and Ammeter to read the current through the lanes, by using this we will characterize the channels/ lanes. This is the main drawback of the old setup and to overcome this designers going for the new setup.

Disadvantages of Old setup:

- It will take more time to complete the validation process
- The more expensive of the Keithley switch
- Area of the setup
- Time to market will be more
- Additional use of the Voltage source and DMM
- Less accuracy in the results
- Less automation process
- The signal loss through the trace path and switch.

III. PR0POSED METHODOLOGY

The old methodology have some disadvantages that already mention above, to overcome that drawbacks designers are looking for the new methodology with new setup as shown below,

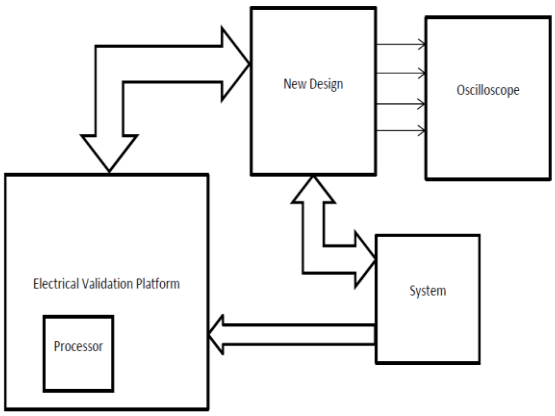

Figure 3.1: The Block Level Representation of the Proposed Methodology.

The above figure 3.1 shows that the block level representation of New Methodology with New design, here it is replacing the Keithley Switch, Voltage source and DMM with NEW DESIGN. The new design contain mainly two parts,

1. Hardware part
2. Software part

The hardware part is replacing the Keithley switch, Voltage source and DMM. And the software part is used to interlink the Hardware part with Server System, Platform and Oscilloscope. Here we are using Python Scripting tool, we will discuss about this in later chapters.

IV. HARDWARE DESIGN

The physical part in the new design is also called as Hardware part. It is very important step in the project, here we need to understand the analog concepts well and we need to know about internal setup of the old methodology then only we are comfortable to start the new design. It contain two major parts, they are

1. Central Board
2. Side Board

Keenly observe the below figure 4.1, it shows the difference between the central board and side board. In our design it contains ONE central board and FIVE side boards.

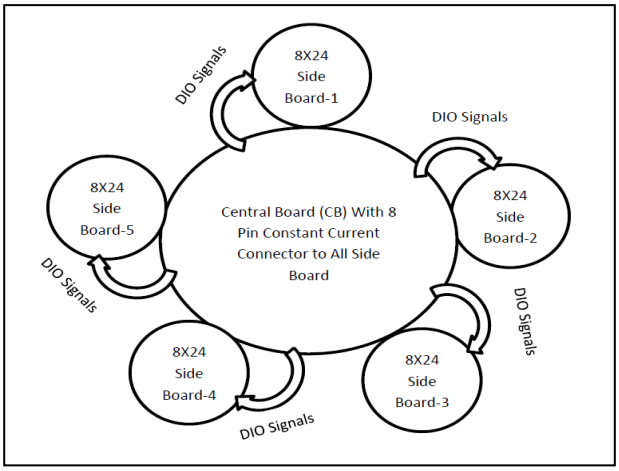

Figure 4.1: Block level Representation of Actual Design.

Here all the side boards are communication with the central board with 8 pin bus connector, and with some Digital IO pins to control that side boards.

Central Board

Here the Central board is replacing the Keithley switch, VS and DMM setup so that the area and cost is reduced than the old design. In this it contain two separate parts as

a. NI-DAQmx-6008

b. Bipolar Constant Current Source circuits

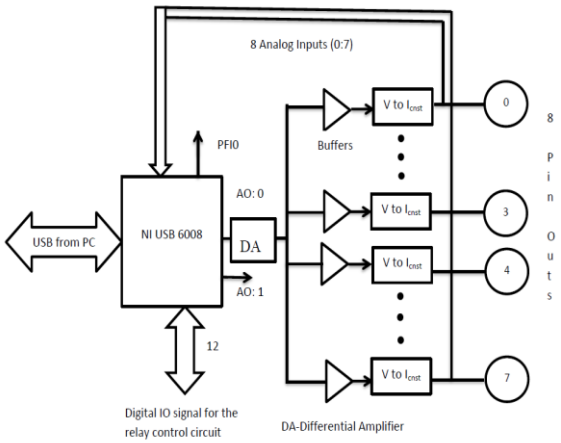

Figure 4.2: Central Board.

To calculate the output current expression we need to consider some assumptions as all the resistor's are precision resister's, and R1=R6, R2=R5, R3=R4. If you calculate the I-Constant at this condition's the output will be as follows,

I-Const = [(R2+R3)/(R1*R3)]*V-diff

Where, I-Const: Bipolar Constant Current Output

R1, R2, R3: Precision Resistors

V-diff: Differential Input of Voltage to I-Const converter

Side Board

The side board is user to replace the Keithley switch setup. This contains relay circuitry, each board is act like a 3X1 MUX with the width of "8" (lanes). It means 24X8; out of 24 lanes it will activate 8 lanes. To control this we are using 2:4 decoders, the decoder contain 3 inputs one is EN, I1 and I2. Where all inputs are coming from Digital IO signals of NI-6008.for every board one single Enable Signal so total 5 DIO signals + 2 DIO common input to all Decoders in all Boards. The 24 lanes are connected from the EV platform that is connected to the central board through Relay circuitry. But only 8 lanes are able to connect to the CB (Central Board). So we need to select the 8 lanes out of 24 lanes, for that we are using the 2:4 decoder. It contain two common inputs to select one of the relay circuit out of RC <1…7>, RC<8…15>, RC<16…23>,

Where RC = Relay Circuit.

DIO-j is act like an enable signal to enable one side board out of all five boards. Then finally we can control the side board using DIO of NI-6008. To control this we have one automation method by using Python scripting. it is possible to find the parameters for different inputs of currents and possible to save the resultant data into an excel file and then store that resultant file in the desired location. Then analyze the data and compare with designers spec.

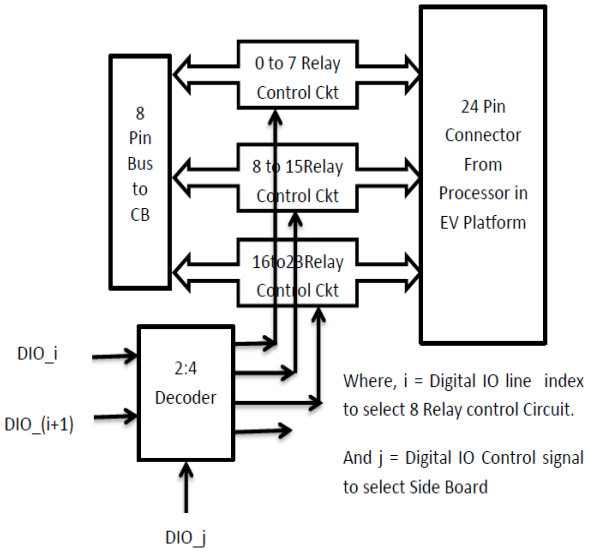

Figure 4.3: Block Diagram of Side Board.

V. SOFTWARE DEVELOPMENT

The software part is used to control the Hardware part, there are many scripting tools available, but best scripting language is PYTHON language. It is easy to understand and easy to program. But here it needs some other packages to communicate with NI-DAQmx-6008. So first we need to install NI-DAQmx software in our system then we will start controlling. There are two ways of controlling,

1. GUI control
2. Control through the Commands

The GUI control will increase the complexity of the work so it is better to select Control through the commands. Here the execution is automated through the python script, so the more automation is possible in this case.

VI. HARDWARE SOFTWARE CO-DESIGN

The interfacing of the Hardware with the System using Python is very important step in this project. By using

NI-6008 we are controlling the remaining parts in the hardware, but internally the python script is using to control that NI device. After installation of the NI-DAQmx software start to control the NI device first then we can set the desired input voltage to the circuit through the NI device.

NI-DAQmx

The NI-DAQmx driver software is one of the layers of software. This is used for easily communicating with the hardware parts. It forms the intermediate layer between the hardware and the application software. Driver software also protects a programmer from having to do register level programming commands in order to control the hardware functions.

VII. RESULTS AND INFERENCE

The cost and the execution time are the main parameters to choose this project by the designers. The below table 8.1 indicates how this project is appropriate to increase the performance with respect to the cost and speed from the old design. And the speed is almost increased by a factor of 8. The below table 8.1 contain the execution time and cost comparison in both cases.

Number of Pins per switch	Total Cost in $ before new design	Total Cost in $ after new design	Execution Time before the new design	Execution Time after the new design
16	1000	320	16	2
32	2000	640	32	4
48	3000	960	48	6
64	4000	1280	64	8
72	5000	1440	72	9

The variation in the time spent and the cost is given in the different plots as below. The Execution Time variation from old design to new design is given by following graph,

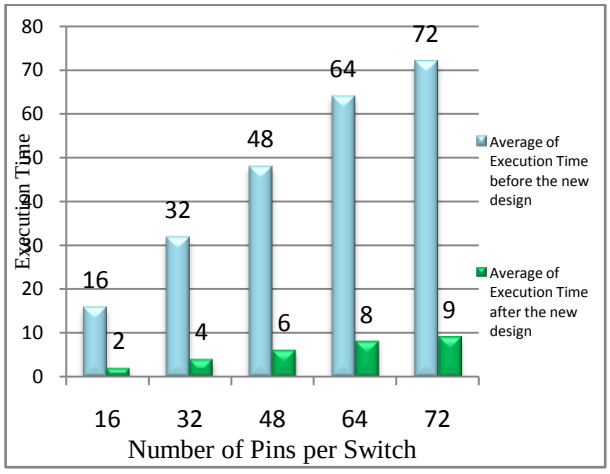

Figure 7.1: Comparison of Results in terms of Execution Time.

The Total Cost variation from old design to new design is given by following graph,

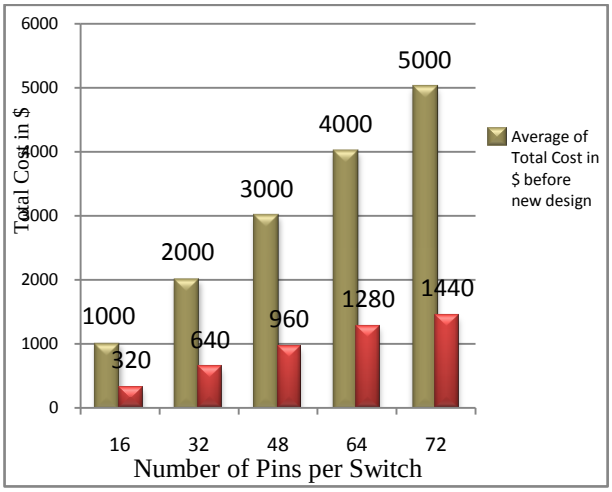

Figure 7.2: Comparison of Results in terms of Total Cost in $.

Advantages of the Proposed Methodology

- It will take less time to complete the validation process
- The more expensive Keithley switches are replaced by the new design with low cost
- It reduces the area of the setup
- Time to market will be less
- Additional use of the Voltage source and DMM are replaced by NI-DAQ-6008
- More accuracy in the results because of NI device
- The total Validation process is automated using the new design and the Python script.
- Less signal degradation through the signal path and switches than old design in old design it contain 3 stage relay circuit now it is reduced to single stage relay circuit.
- No need of extra-power supply to the NI 6008 device

VIII. CONCLUSION AND FUTURE WORK

Post-Silicon validation and debug process begins with the arrival of prototype silicon and can continue well after product has gone into production. It is most exciting and challenging stage of integrated circuit development process. The main purpose of debug is to identify and resolve any bugs in silicon to ensure that silicon operates correctly for customers over the specifications. Post-silicon validation has become

increasingly important to qualify products, because design does not fully account for many parameters impacting the silicon performance. Designing for worst case or adding guard band can lead to unacceptable power/performance.

Because of the proposed methodology have more advantages than the old methodology. It increases the speed of the execution by the automation scripting, and rapidly reduce the cost of the design than previous version. And the area consumed by the proposed design.

Future Work

Presently it is using for Transmitter Characterization of the processor; we can extend it for the Receiver Characterization also with some enhancements in this project. And we can increase speed by replacing the NI-6008 with NI USB 62XX series with more AI pins.

IX. REFERENCES

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