Reduced Comparator Flash ADC for ECG Applications


Department of Electronics and Communication Engineering,
Angel College of Engineering and Technology, Anna University of Technology, Tirupur, Tamil Nadu
E-mail : akshaya.th23@gmail.com, ushab1991@gmail.com, prakash3192@gmail.com, sukirtharaj.b@gmail.com

Abstract – A CMOS based 4-bit Flash Analog to Digital Converter (ADC) design with reduced number of comparators than the conventional Flash Analog to Digital Converter and multiplexer based architecture is proposed. For improving the conversion rate, both the analog and digital parts of the ADC are fully modified and the architecture uses only 4 comparators instead of 15 as used in conventional flash ADC, thus saving considerable amount of power. The proposed 4-bit ADC is designed and simulated in TANNER tools with 1.2 V supply voltage using TSpice simulation.

Keywords – Flash ADC, Comparators, CMOS, TANNER, TSpice.

I. INTRODUCTION

The performance of biomedical data acquisition systems such as ECG is generally limited by precision of the digital input data, which is achieved at the interface between analog and digital signals. ECG is a common bio-potential signal with low amplitudes of 1000-10000 µV and low frequency of 0.5-100Hz [1]. In ECG applications the design with minimum power dissipation is always the key while fabricating the integrated circuit for such an ADC. The main problem of flash ADC architecture is that they consume much power and the complexity of the design increases proportionally with the resolution.

Successive approximation architectures which have a logarithmic dependence on resolution are alternative approaches to reduce the complexity and the power consumption of flash ADC. On the other hand, it’s not desirable to use those kinds of ADCs in high-speed applications since they consume multiple clock cycles to implement the conversion algorithm, which needs more time interleaving to increase the conversion speed.

The main concern of this paper is to reduce the power consumption for flash ADC to be suitable for usage in low voltage applications. Flash ADCs are still the architecture of choice, where maximum sample rate and low to moderate resolution is required [9]. Speed, resolution and power dissipation are the three main parameters for ADC [5] and they can’t be changed once an ADC is designed. This paper presents a CMOS based 4-bit ADC that uses only 4 comparators instead of 15 comparators so it dissipates minimum power and can operate at higher speed at low resolution. This paper is organized into 5 sections.

The conventional flash ADC is reviewed in Section II. The proposed flash ADC architecture is presented in Section III. Simulation results are demonstrated in Section IV. Conclusions are drawn in Section V.

II. CONVENTIONAL FLASH ADC

A block diagram of a conventional N-bit flash ADC is shown in Fig.1. For an N bit Flash Analog to Digital converter the circuit employs \(2^N - 1\) comparators. A resistive divider with \(2^N\) resistors provides the reference voltage. These voltages are compared with the analog input signal in just one clock cycle. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a "1" when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is "0". These voltages are compared with the analog input signal in just one clock cycle.

The encoder is used to convert the thermometer code, generated by the comparators into a binary code that approximates the input signal. The cyclic encoder
detects the pair of 1-0 and 0-1 location and converts it to binary.

Fig. 1 : Block diagram of conventional N-bit flash ADC

III. PROPOSED FLASH ADC ARCHITECTURE

The block diagram of proposed 4-bit flash ADC is shown in Fig.2. It uses multiplexer and reduced number of comparator for ADC operation. The multiplexer is used for generation of reference voltages while the comparators are used for comparing different reference voltages.

In comparison to the conventional flash ADC which uses $2^{N-1}$ comparators for N-bit ADC, the proposed one uses only N comparators and N-1 multiplexers to generate the required binary code resulting in saving of power and area.

The principle behind this proposed work is to use analog multiplexer to change the reference voltage in accordance to the previous significant bit and to exploit the properties of comparators. As comparators are the fast element and consume most of the power hence to reduce the power, the reduction of comparators is the only alternative and the proposed design follows the same path.

The most significant part of ADC architecture is comparator. Comparator is a circuit that compares two analog input signals and decodes the signal into single digital output signal. Flash type ADC usually referred as direct conversion ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. Direct conversion is very fast, capable of gigahertz sampling rate. The schematic design of comparator is shown in Fig.3. The input voltage is compared with the reference voltage and the output is 1 when input voltage is greater than the reference voltage. Output is 0 when input voltage is lesser than the reference voltage.

Fig. 2 : Block diagram of 4-bit flash ADC

If the input step is sufficiently small the output should not slew and the transient response will be a linear response. The settling time is the time needed for the output to reach a final value within a predetermined tolerance, when excited by a small signal. Small-signal settling time is determined by the gain bandwidth product of the amplifier.

If the input step magnitude is sufficiently large, the comparator will slew by virtue of not having enough current to charge or discharge the compensating and/or load capacitances. The slew rate is determined from the slope of the output waveform during the rise or fall of the output. Slew rate is limited by the current-sourcing/sinking capability in charging the output capacitor.

In comparator there are two stages, first stage is composite cascode differential amplifier N channel input devices in series with combination of cascode active PMOS based current mirror load that compares the two input but provide smaller gain while the second stage is common source provide larger swing and
greater gain similar to opamp based conventional two stage open loop comparator and one NMOS is provided below which act as current sink for stabilization. Amplifiers are usually employed to achieve linear operation in closed loop configuration which requires careful compensation to avoid unstable operation. On the contrary the comparator does not require stability criteria as in two stage amplifier so it eliminated need for compensation capacitor.

A CMOS inverter is one of the key elements of multiplexer [10]. The inverter includes a p-type MOS transistor and an n-type MOS transistor. Gate terminal of PMOS and NMOS are connected in common to serve as input terminal. Drains of PMOS and NMOS are connected in common to serve as output terminal. The multiplexer comprises of transmission gates which make the multiplexer non-restoring. Transmission gate consists of NMOS and PMOS connected in parallel. The input terminal of the gate is composed by source terminals of the transistors PMOS and NMOS connected in common. The output terminal of the transmission gate is made of drain terminals of PMOS and NMOS also connected in common. Selection signals S and S’ are applied to gate terminals of PMOS and NMOS transistors respectively. The select signal S and its complement S’ can enable simultaneously one of the two transmission gates at any given time when both the PMOS and NMOS transistors of the gate are on. The magnitude of input signals is substantially similar to value of Vdd or Vss when logic 1 or logic 0 respectively is applied to the input terminals. Fig.4 presents the schematic of 2to1 multiplexer. This multiplexer is preceded by a set of three NMOS transistors (M1, M2 and M3) for providing the input (V/4 and 3 V/4) to the 2to1 multiplexer which is required for 2to1 multiplexer as can be seen from Fig. 2.

For providing different reference voltages to the comparator, CMOS based transmission gate is used as analog multiplexer. Multiplexers are key components in CMOS memory elements and data manipulation structures. A multiplexer chooses the output from among several inputs based on a select signal. The conventional multiplexer has at least two inputs, at least one output and at least one control select line terminal. Each of the inputs is associated with a separate and distinct path through the multiplexer. One source terminal of the multiplexer circuit is connected to high voltage source Vdd. Another source terminal is connected to ground or Vss. The conventional multiplexer are mostly built in complementary metal-oxide-semiconductor technology to perform logic functions. The CMOS-based multiplexers have leakage power that tends to increase with a reduction of their dimensions. The conventional multiplexers are volatile; they can lose their logic states when the power is off. The choice of employing transmission gates in preference to pass transistors is because of its effect on dynamic range.
The schematic design of 8 to 1 multiplexer is shown in Fig.6. It requires eight inputs and three selection lines.

The dc transfer analysis is shown in Fig.8. The change in output voltage with respect to input voltage is observed at minimum voltage of 0.4V and at maximum voltage of 3.2V.

The proposed flash ADC is implemented in 0.18µm technology and simulated using Tanner T-SPICE simulator. The design operates at 1.2V supply voltage. Fig.7 shows the simulated waveform of comparator. Fig.9, 10, 11 shows the simulated waveform of 2 to 1 multiplexer, 4 to 1 multiplexer and 8 to 1 multiplexer respectively. It can be seen that the output rises by one LSB when any one of the selection line is active.
The simulated output of proposed ADC architecture for sine input of 128MHz is shown in Fig.12. The sampling rate is 2Gs/s. The power dissipation is about 2.15mW. Comparison is drawn between different types of flash ADC’s as shown in TABLE I.

![Fig.9: Simulated waveform of 2 to 1 multiplexer](image1)

![Fig.10: Simulated waveform of 4 to 1 multiplexer](image2)

![Fig.11: Simulated waveform of 8 to 1 multiplexer](image3)

![Fig.12: Simulated output of proposed ADC](image4)

TABLE I

<table>
<thead>
<tr>
<th>ADC Type</th>
<th>Proposed</th>
<th>[6]</th>
<th>[7]</th>
<th>[8]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>4</td>
<td>3</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>Technology</td>
<td>0.18μm</td>
<td>0.18μm</td>
<td>130nm</td>
<td>0.25μm</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>2Gsps</td>
<td>-</td>
<td>2.5Gsps</td>
<td>555Mfps</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.2V</td>
<td>1.3V</td>
<td>1.2V</td>
<td>2.5V</td>
</tr>
<tr>
<td>Power</td>
<td>2.15mW</td>
<td>36.27mW</td>
<td>23.77mW</td>
<td>11.58mW</td>
</tr>
</tbody>
</table>

V. CONCLUSION

A 4-bit ADC with reduced comparator is designed and simulated using 0.18μm CMOS technology. The proposed architecture operates at a low voltage of 1.2V and consumes only minimum power of 2.15mW. The architecture with reduced number of comparators makes it useful in portable ECG systems which operate at low voltage and at low frequency range.

VI. ACKNOWLEDGMENT

The authors would like to acknowledge the help of Mr. V. A. SARAVANAN, B.E., M.Tech., (PhD), Assistant Professor, Department of Electronics and Communication Engineering for providing innovative suggestions, scholastic advice and unstinted guidance at every stage.
VII. REFERENCES


