Design and Comparative Performance Analysis of 1-T DRAM Cell with Nanoscale SOI and MOS Structures

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Abstract - Presently, low power device design and implementation have got a significant role to play in VLSI circuit design. VLSI circuit efficiency, either memory or processor, can be significantly improved through a combination of device scaling, new device structures and material property improvement to its fundamental limits. Since, conventional silicon technology has been suffered from the fundamental physical limitations in the sub-micron or nanometer region, some alternative device technologies like Silicon-on-Insulator (SOI) technology has been emerged. Transistor scalability and circuit performance are improved through significant reduction in Short-Channel-Effects (SCEs) by using ultra-thin, fully depleted Silicon-on-insulator (SOI) technology. Till now intense interests have been paid in practical fabrication and compact modelling of SOI MOSFET but little attention has been paid to understand the circuit performance improvement with SOI compared to bulk MOSFET, especially in the domain of semiconductor memory design. In the present analysis, one transistor DRAM cell has been designed with SOI and conventional MOSFET using TCAD Simulator. DRAM reading and writing operations have been compared to implicate the improvement in efficiency with SOI technology. Time delay along with the power consumption issue has been comparatively analysed. It has been observed that SOI DRAM cell shows better reading sensitivity as well as better power efficiency compared to MOS DRAM cell.

Keywords - DRAM, SOI MOSFET, Compact Model, SPICE, Leakage Current, Power Dissipation.

I. INTRODUCTION

After the introduction of the first commercial MOS RAM chips, memory chips have been demonstrated more than 1 million times hike in storage capacity per chip during last few decades [1]. The circuit that initiated this incredible capacity increase of memory chips is called the one-transistor dynamic RAM or 1-T DRAM [2]. Presently 1-T DRAM is the most common kind of random access memory for mobile/personal computers, workstations and many others electronics gadgets and equipments [3]. A 1-T DRAM cell of present era has a very simple structure, which is composed of one transistor and one capacitor per bit. Compared to six transistors Static RAM (6-T SRAM) cell based memory chip, 1-T DRAM cell based memory chip can achieve very high integration density and thus tremendous storage capacity [4-5]. In practical DRAM cell, capacitors and transistors suffer from charge leakage, thus the information eventually fades unless the capacitor charge is refreshed periodically which makes DRAM less power efficient [6-7]. But such power problem can be minimized by addressing different design issues of DRAM cell especially reducing the leakage through MOSFET structure itself [8-9].

Till now major performance improvement of MOS based 1-T DRAM cell has been achieved by increasing the speed and decreasing, both the power consumption and size of MOS [8-9]. As scaling of planar MOS has been facing significant challenges, several non-conventional geometry MOS structures have been studied experimentally as well as theoretically in recent time [9]. Among the non-conventional structures, silicon-on-insulator (SOI) technology has received much attention of the researchers due to some of its inherent advantages [10]. The SOI technology offers many advantages over silicon based conventional MOS technology, in particular, higher speed, high radiation tolerance, lower parasitic capacitance, lower short channel effects, better current deliverability, manufacturing compatibility with the existing technology [11-13]. SOI MOSFET suffers from less leakage current [13-14] compared to conventional MOSFET which can give significant advantage in designing power efficient DRAM cell.
Intense research on practical fabrication and compact modelling of SOI MOSFETs have been carried out during last few decades but little attention has been paid to understand its attributes in memory design [14]. But to understand the true potential of SOI MOSFET as a next generation memory component, SOI MOSFET based memory cell analysis is essential. Therefore, in the present analysis 1-T DRAM cells have been designed with S-SPICE (from SILVACO), with latest nano-scale compact models of SOI and MOS. Simulations are carried out to compare the efficiency and accuracy in writing/reading operation and comparative power analysis for both the structures.

II. SIMULATION MODEL

Presently, the third generation of BSIM model has been widely used by most semiconductor and IC design companies world-wide for device modelling and CMOS IC design [15]. In present analysis, for conventional MOS DRAM circuit, latest fourth generation BSIM4 (verilog-a version) model has been used [16]. For SOI DRAM circuit, very recently developed BSIMSOIv4.4.va model has been used [16]. Firstly, schematic has been designed with GATEWAY simulator of SILVACO and then generated spice code has been executed in SMART SPICE with the incorporation of verilog-a model for MOS and SOI DRAM cell, respectively. A generalized 1-T DRAM circuit indigenously designed for reading and writing operation, has shown in Fig. 1.

III. CIRCUIT OPERATION

Present memory circuit has ingeniously designed for executing both reading and writing operation with the same circuit setup.

**Writing operation:** It starts with zero charge across the DAM capacitor C1. Now first, M1 has to be switched on (through V3 supply) to write data in the DRAM or to charge the capacitor C1. Now M2 will be switched on (through V2 supply) and data will be written in memory cell through supply V3 and C1 will be fully charged or DRAM will store ‘one’. All the supplies here are taken as a square pulse generator with variable ‘on’ and ‘off’ time based on requirements of the present analysis.

**Reading Operation:** To read data, first M1 is switched off (holding state of DRAM), M2 is switched on and then C2 is charged to half of the supply voltage (VDD/2) through V1. Now M2 will be switched off to cut off any discharging path for C2. Now M1 will be switched on and there will be charge transfer between C1 and C2. If C1 is holding ‘0’, voltage across C2 will be reduced by some factors from VDD/2 and it will be reverse if C1 is holding ‘1’. So, by sensing the voltage change across the capacitor C2, data can be read out from the DRAM cell.

IV. RESULT & DISCUSSION

Simulation has been carried out for transistor gate length 100nm, width 500nm, channel thickness 50nm, gate oxide thickness 2nm and other parameters are left as default as in the model cards of the simulator.

![Fig. 1: Schematic of DRAM cell with peripheral circuitry for writing and reading operation.](image)

![Fig. 2: Timing diagram of different input square pulse supplies used in present circuit simulation.](image)

![Fig. 3: Timing diagram for writing analysis; voltage across the capacitor C1 for MOS (top) and SOI DRAM (bottom).](image)
Writing analysis starts with zero across DRAM capacitor C1 and charging of C1 signifies successful writing (state ‘1’) operation. Comparing the above two figures, it is quite clear charging of MOS DRAM takes less time to write data compared to SOI DRAM and output ‘high’ voltage is also little less for SOI DRAM, which initiates better noise margin for MOS DRAM writing operation. But MOS DRAM suffers from high leakage current as soon as writing signal shifts to zero, at 10ns; there is significant reduction in C1 voltage compared to almost no voltage change of SOI DRAM. This effect attributed from less substrate leakage current associated with SOI compared to MOS [12]. For SOI based DRAM, the rise time is around 3-4 times higher the MOS based DRAM and this may be attributed by the RC delay in SOI MOSFET initiated with higher ‘on’ resistance of compared to conventional MOSFET [13].

Reading analysis starts with ‘one’ state across DRAM capacitor C1 and charging of C2 with half V_{DD}/2 and then opening every other transistor switches in the circuit except M1 which will allow charge transfer between DRAM capacitor C1 and virtual bit line capacitor C2. Change in the voltage across C2 will represent the state of the DRAM; voltage shift above V_{DD}/2 will establish successful reading of ‘one’ and down shift from V_{DD}/2 will be read as ‘zero’. From the Figure-4, it’s quite visible that, in SOI DRAM the reading operation is more prominent compared to MOS DRAM, in terms of sensitivity. SOI DRAM produces 0.5V shift in voltage across C2 compared to 0.15V shift in MOS DRAM which initiates better noise margin for SOI DRAM reading operation. This may be caused by lose of charge (in C1) through leakage in case of MOS DRAM. Significantly MOS DRAM reading operation is 2 time faster then SOI DRAM and such RC delay may be caused by higher ‘on’ resistance of SOI MOSFET.

![Timing diagram for reading analysis: voltage across the capacitor C2 for MOS (top) and SOI DRAM (bottom).](image)

<table>
<thead>
<tr>
<th>Type Of DRAM</th>
<th>Static Power</th>
<th>Dynamic Power</th>
<th>Switching Power</th>
<th>Total Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional MOSFET</td>
<td>0.5</td>
<td>18</td>
<td>0.625</td>
<td>18.630</td>
</tr>
<tr>
<td>SOI MOSFET</td>
<td>0.2</td>
<td>9.02</td>
<td>0.694</td>
<td>9.114</td>
</tr>
</tbody>
</table>

Table 1: Power (in mW) calculation of MOS and SOI based DRAM.

Over all power calculation of SOI and conventional MOS based DRAM have shown in the Table 1. It is clear form the present analysis under the present structural and operational considerations, SOI based DRAM consumes less overall power then MOS based DRAM.

V. CONCLUSION

Under present analysis, a 1-T DRAM memory cell has been designed and analysed using SOI and conventional MOSFET to realize the potential improvement in memory cell design with nano-scale SOI MOSFET. By comparing the simulated results of proposed and existing model, it has been found that the time delay is little higher for writing and reading operation with SOI DRAM compared to MOS DRAM which will make SOI DRAM little slower then MOS DRAM. But significant improvement can be achieved with SOI DRAM in-terms of power as it will require less frequent refreshing due to lower leakage current. Reading is also prominent for SOI DRAM as higher sensitivity can be achievable with prominent voltage.
shift in bit line. The time delay issue related to higher on resistance with SOI can be addressed with the modification in structural parameters at the design and fabrication level and doing so, SOI DRAM can be a better candidate for future nano-scale, ultra dance IC memory chip.

VI. REFERENCES


