Enhanced Tolerant Permanent Faults in FIFO Buffers of Network on Chip Routers using Bench Mark Circuits

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Abstract : A solution for communication bottleneck is the use of an embedded switching network, called Network-on-Chip (NoC), to interconnect the IP modules in Systems-on-Chip (SoCs). Hence this research model of the proposed algorithm to run the test periodically to prevent the accumulation of repetitive tests, the router technique involves been integrated into the channel interface and on-line testing has been performed with data traffic, such as synthetic self. In addition, routing logic an on-line test technology for the transportation of samples to test, using the title proposed flits the data traffic movement.

I. INTRODUCTION

The hardware used in this paper is the basic input for the production of a sequence of linear feedback shift register (LFSR) on a random basis and a small number of gates (almost every one of the six gates of the benchmark circuits that need to be considered). Repeat the sequence of gates gained the same or similar in order to avoid cases where states take to the circuit to be used for random order. The repeated synchronization referred to as. In addition, on-chip test circuit is applied to the generation of the hardware is based on the tests used to determine a single gate. As a result, it is compatible with the following parameters given by the circuit is a simple and fixed hardware architecture is.

1. LFSR number of bits.
2. The length of the primary input sequence.
3. Changing the order of the specific gates used for the LFSR sequence.
4. Based on a specific gate circuit is applied to the functional tests used for selecting a broadside.
5. The basic input sequences and many sub-tests in order to produce seeds for the LFSR.

Pseudorandom bit generator is presented. It is based on a shift register with a dynamic linear feedback, which, compared to the linear feedback, improves its inviolability property. The proposed circuit exhibits statistical characteristics similar to a linear feedback pseudorandom bit generator with equivalent length [1].

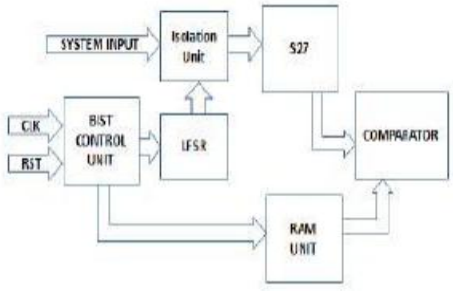


Fig1.1 Simple BIST circuitry.

II. LITERATURE SURVEY

In [2], shortest linear feedback shift register capable of generating a prescribed finite sequence of digits. The shit-register approach leads to a simple proof of the validity of the algorithm as well as providing additional insight into its properties. The equivalence of the decoding problem for BCH codes to a shit-register synthesis problem is demonstrated, and other applications for the algorithm are suggested.

The discussion of linear recurring relation whose characteristic polynomial is primitive, was fond out the number of possible realisations using Linear Feedback Shift Registers (LFSRs) with 2-input 2-output delay elements [3]. The results show the equivalence between each realisation and a matrix having a special structure. Further, the number of realisations is computed by calculating the number of these structured matrices.

A dynamic linear feedback shift register (DLFSR) for cryptographic application. The particular topology there proposed is now analyzed, allowing us to extend the results to more general cases. Maximum period and linear span values are obtained for the generated sequences, while several estimations for autocorrelation and cross-correlation of such sequences are also presented. Furthermore, the sequences produced by DLFSRs can be considered as interleaved sequences. This fact allows us to apply the general interleaved sequence model proposed by Gong and consequently simplify their study. Finally, several remarks are stated regarding DLFSR utilization for cryptographic or code division multiple access (CDMA) applications [4].

This study in [5] based on the injection of resistive defects as their presence in VDSM technologies is more and more frequent. Electrical simulations have been performed to evaluate the effects of those defects in terms of detected functional faults. Read destructive, deceptive read destructive and dynamic read destructive faults have been reproduced and accurately characterized. The dependence of the fault detection has been put in relation with memory operating conditions, resistance value and clock cycle, and the importance of at speed testing for dynamic fault models has been pointed out. Finally resistive Address Decoder Open Faults (ADOF) have been simulated and the conditions that maximize the fault detection have been discussed as well as the resulting implications for memory test.

The NoC core testing problem is formulated [6] as a unicast-based multicast problem in order to reduce test data delivery time in the NoC. Test response data are forwarded back to the automated test equipment (ATE) via the communication channels using the reverse paths of test data delivery, which are compacted on the way from each processor to the ATE. A new power-aware test scheduling scheme is proposed, which is extended to cases for multiple port ATEs. Test data is further compressed before delivering and a low-power test application scheme is used for the cores because power produced by cores is the bottleneck of NoC test. Experimental results are presented to show the effectiveness of the proposed method in reducing the NoC test cost and test data volume by comparing to the previous methods.

The work in [7] present a fault-tolerant approach based on using the shortest paths. This method maintains the performance of Networks-on-Chip in the presence of faults. To avoid using non-minimal paths, the router architecture is slightly modified. In the new form of architecture, there is an ability to connect the horizontal and orthogonal links of a faulty router such that healthy routers are kept connected to each other. Based on this architecture, a fault-tolerant routing algorithm is presented which is obviously much simpler than traditional fault-tolerant routing algorithms.

III. EXPERIMENTAL RESULTS

A prototype implementation of the proposed test circuit has been integrated into the router-channel interface and online transparent SOA-MATS++ test is performed with synthetic self-similar data traffic. The router design considered in this brief has been taken from.

Modelsim and Xilinx Tools

At the beginning of the semester, we will focus on getting acquainted with the VHDL syntax. We will use ModelSim 5.7 to simulate and verify the functionality of our VHDL code. This tutorial teaches the basic capabilities of ModelSim.

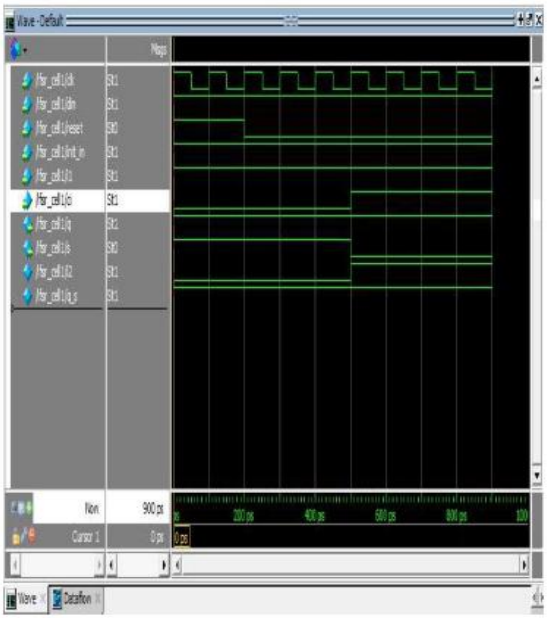


Fig: 3.1 LFSR cell design

Area Overhead Estimation of the Test Hardware

The proposed hardware for the test circuit described in Verilog HDL and support for Synopsys Design Vision has been synthesized using 90 nm CMOS technology. After the synthesis of the various modules in the test circuit is expected to total area of the FIFO buffer area (have a depth equal to 6), however, is estimated to be 4074 μm2, ~ 1720 μm2 predicted. Therefore, the results of the test circuit is a significant amount of overhead due to the inclusion of 42%.

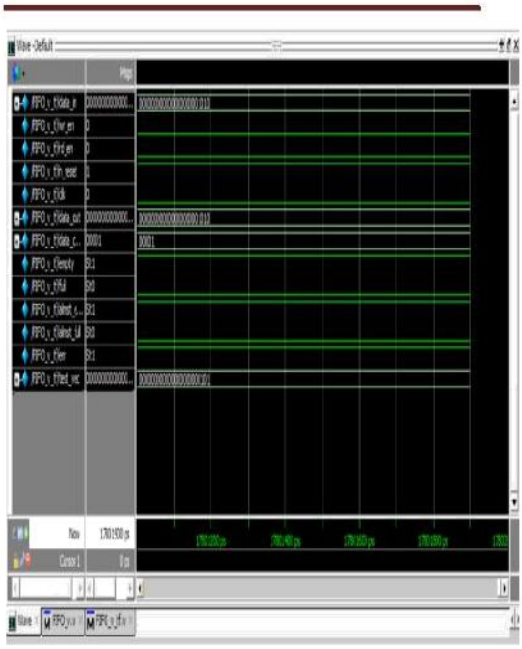
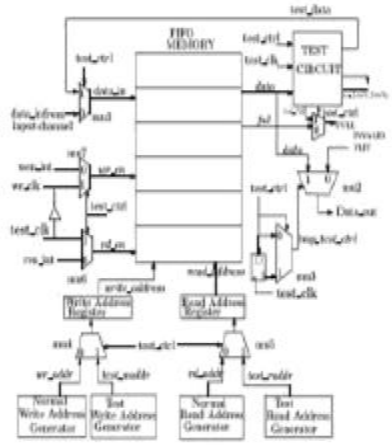


Fig:3.2 Waveform for FIFO withoutFaults

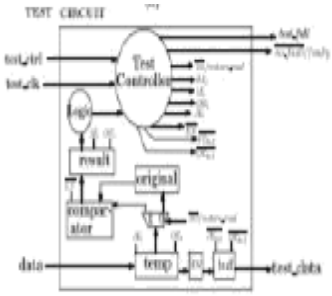
Table 1. The output of LFSR.

U	LFSR(u)
0	101 011 100 100

1	010	101	110	010
2	101	011	100	100
3	100	101	011	100
4	010	010	101	110
5	001	001	010	111
6	100	100	101	011
7	110	010	010	101
8	111	001	001	110
9	011	100	100	101
10	101	110	010	010
11	010	111	001	010
12	001	011	100	101
13	100	101	110	010
14	010	010	111	001
15	101	001	011	100



(a)



(b)

Fig 3.3 Test generation logic for a group

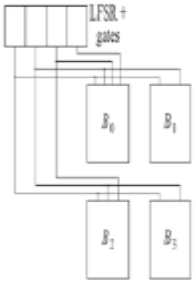


Figure 3.4 Hardware implementation of the test process for the FIFO buffers. (b) Implementation of test circuit.

Test Architecture

Each input channel of an NOC router SRAM based FIFO memory in the FIFO buffer is present in some depth. During normal operation, the data buffer will come through a data_in line and then are stored in different parts of the FIFO memory flits.

The test, enable and disable the test writing is synchronized with the clock. As mentioned before, the alternative of a test at the edges of the clock at the time of teperformed read and write operations. If the test is obtained by inverting the clock write_clk read operations, contemporary, positive edges. Test mode (test_ctrl high) generators in the test read and write addresses are generated by the implementation of the test address using the gray code counters similar to the usual address generation. Muxes M4 and M5 is used to select between common addresses and test addresses.

IV. CONCLUSION

In this research SRAM FIFO memories are based on the development of a transparent run-time permanent faults SOA- mats ++, test generation algorithm is proposed to detect. NOC proposed transparent test and periodic testing of the routers used to handle inside the FIFO memory. Periodic testing of the buffers and buffer to prevent the accumulation of faults to test each location. FIFO buffers the periodic examination of the results of the simulation tests of buffers, very often, except when the total throughput of the NOC does not have much effect on the show.

This work also performed the buffers simultaneously with the test sample for the encoding of the data packets used in the fields of flits title would be the use of an online testing technology for the proposed routing logic. In the future work, we continued testing of incoming data packets to a router under test and would like to modify the proposed FIFO testing technology.

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