10 nm, 7 nm and Beyond Technologies

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Abstract-- The whole purpose of the paper is to give a glimpse of the new technologies that are being used by the leading chip manufacturers such as Intel, Samsung, Global Foundries, etc., to compare these technologies, discuss their limits and conclude with the further growth. Moore's law is the observation that the number of transistors in a dense integrated circuit doubles approximately every two years. Demand, which in turn has some serious problems for the semiconductor industry, following a deviation from Moore's Law. The building block of computer processors is the transistor. Which is nothing more than a gate which either allows electrons to pass – or doesn't depending on the state. When we talk about the process node getting smaller – it is actually these gates which are getting smaller. A gate below 7nm will be just a few silicon atoms thick (1 nm has about two silicon atoms but the process name does not correspond directly to the size of the gate).When dealing with gates this small an interesting phenomenon begins to occur – the electron can simply chose to be on the other side of the gate; in other words they can effectively tunnel through the closed transistor and appear on the other side. And when you are talking about logic sensitive circuits, you can't have closed gates leaking electricity.

Keywords: CMOS, VLSI, finFET, EUV (Extreme Ultra Violet), Lithography, MOSFET.

I. INTRODUCTION

The growing packing density and power consumption ofVLSI (Very Large Scale Integration) circuits have made thermal effect an increasinglyimportant concern of VLSI designers. The need to reduce power consumption in VLSI circuits and meet thermal constraints is driving the push toward ultra-voltage scaled CMOS (Complementary Metal-Oxide Semiconductor) designs, i.e., circuits that operate at near/sub-threshold supply voltage levels. The rapid pace of technological progress would not have been possible without satisfactory improvement in long term reliability of circuits. Despite significant challenges, circuit reliability has been maintained, preventing it from constraining the rate of scaling. In semiconductor manufacturing, the International Technology Roadmap for Semiconductors defines the 7 nanometer (7 nm) node as the technology node following the 10 nm node. Single transistor 7 nm scale devices were first produced in the early 2000s – as of 2017 commercial production of 7 nm chips is at development stage. In the semiconductor fabricationmethod, the International Technology Roadmap for Semiconductors (ITRS) defines the 10 nanometer (10 nm) node as the technology node following the 14 nm node. "10 nm class" denotes chips made using process technologies between 10 and 20 nanometers. Samsung first released their version of a "10 nm" process node in 2017. Also cost is of major concern when it comes to manufacturing of chips on a large scale. With respect to different technologies the cost variations are depicted as shown in figure1 (Courtesy of Intel Inc.). The rest of this paper is organized as follows. Section gives a brief comparison between both 10nm and 7nm technologies, their power consumption and efficiency related information. Section III gives more information about the present industrial scenario of those technologies and their progress. Section IV elaborates the latest processes used in manufacture of those technologies. We discuss the limitations and future scope of other methodologies and technologies in Section V and Section VI.

Figure 1: Cost estimations in each scenario. (Courtesy of Intel Inc.)

II. BRIEF COMPARISON

10nm brings a lot of benefits to our customers in terms of area scaling, performance and power. So overall, the power improvements are very substantial compared 14nm. We have compared that in terms of the performance, area and power to 14nm technology. We can see up to a 30% area reduction with a 27% performance improvement or 40% lower power at the same performance. We introduced triple patterning in select ways to make the design more efficient. In theory, 7nm provide better performance than 10nm. 10nm is a robust node, while 7nm will become the more

dominating in the later part of 2017. Compared to 16nm/14nm, 7nm provides a 35% speed improvement, 65% less power, and a 3.3X density improvement. There are power advantages as well as a longer battery life are a few add-on's. Since 7nm is further scaled version of the 10nm, the EUV (Extreme Ultra Violet) lithography technique used in 10nm process will not be sufficient and designers must opt for more complex procedures to realize this technology and implement it.

III. LATEST PROGRESS

In 2012, IBM produced a sub-10 nm carbon nanotube transistor that outperformed silicon on speed and power. The superior low-voltage performance of the sub-10 nm CNT transistor proves the viability of nanotubes for consideration in future aggressively scaled transistor technologies. In April 2015, TSMC announced that 10 nm production would begin at the end of 2016.On 23 May 2015, Samsung Electronics showed off a 300 mm wafer of 10 nm FinFET chips. In August 2016, Intel began trial production at 10 nm.On 17 October 2016, Samsung Electronics announced mass production at 10 nm.On 29 March 2017, Samsung started preorders for their Samsung Galaxy S8 which uses Samsung's version of a "10 nm" processor.As of mid-2016, semiconductor business Intel, and foundries at TSMC, and Samsung were all expected to ship or begin volume production of 10 nm devices in the first quarter of 2017, with foundry customers for 2017 including Qualcomm (Snapdragon 835) at Samsung, and Apple Inc. and MediaTek at TSMC.On 21 April 2017, Samsung started shipping their Galaxy S8 which uses Samsung's version of a "10 nm" processor. At such a nano - level, using of silicon alone can prove to be inefficient. Although Intel has not yet divulged any certain plans to manufacturers or retailers, it has already stated that it would no longer use silicon at this node. A possible replacement material for silicon would be indium gallium arsenide (InGaAs) or graphene.

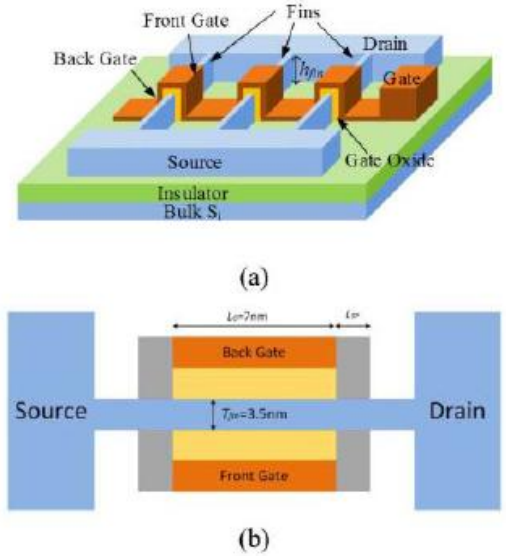

Figure 2 (a) perspective view (b) Top view of a 7nm finFET device

In April 2016, TSMC announced that 7 nm trial production would begin in the first half of 2017. In March 2017, TSMC announced 7 nm risk production starting by June 2018. In September 2016, Global Foundries announced trial production in the second half of 2017 and risk production in early 2018, with test chips already running. In February 2017, Intel announced Fab 42 in Arizona will produce microprocessors using 7 nm manufacturing process. Figure 2 shows the perspective view (a) and the top view (b) of the typical 7nm process on a finFET device.

IV. MANUFACTURING TECHNOLOGIES.

Announced during Intel's Technology and Manufacturing Day 2017, Intel's 10 nm process (P1274) is the first high-volume manufacturing process to employ Self-Aligned Quad Patterning (SAQP) with production starting in the second half of 2017. Intel detailed Hyper-Scaling, a marketing term for a suite of techniques used to scale a transistor, which included SAQP, a single dummy gate and contact over active gate (COAG). Samsung, which uses LELELE (litho-etch-litho-etch-litho-etch), plans ramp up mass production in May of 2017. Due to marketing names, the transistor sizes vary considerably between leading manufactures. For example, Intel's 10nm process is denser and smaller than TSMC's 7 nm process while Samsung's 10 nm process is more similar to Intel's 14 nm process.The 7 nanometer (7 nm) lithography process is a full node semiconductor manufacturing process following the 10 nm process node.Intel announced a $7B investment in Arizona's Fab 42 which will eventually produce chips on a 7 nm process. The 7nm process is still in the development stages and so the manufacturing process is also being developed.

V. LIMITATIONS

While the roadmap has been based on the continuing extension of CMOS technology, even this roadmap does not guarantee that silicon-based CMOS will extend that far. This is to be expected, since the gate length for this node may be smaller than 6 nm, and the corresponding gate dielectric thickness would scale down to a monolayer or even less. Scientists have estimated that transistors at these dimensions are significantly affected by quantum tunnelling. As a result, non-silicon extensions of CMOS, carbon nanotube/nanowires, as well as non-CMOS platforms, including molecular electronics, spin-based computing, and single-electron devices, have been proposed. Hence, this node marks the practical beginning of Nano-electronics. The extensive use of ultra-low-k dielectrics (such as spin-on polymers or other porous materials) means that conventional photolithography, etch, or even chemical-mechanical polishing processes are unlikely to be used, because these materials contain a high density of voids and gaps. At the ~10 nm scale, quantum tunnelling (especially through gaps) becomes a significant phenomenon. Controlling gaps on these

scales by means of electron migration can produce interesting electrical properties. Quantum tunnelling may be advantageous if its effect on device behavior can be understood, and exploited, in the design. Future transistors may have insulating channels. An electron wave function decays exponentially in a "classically forbidden" region at a rate that can be controlled by the gate voltage. Interference effects are also possible;[14]Alternate option is in heavier mass semiconducting channels. Photoemission electron microscopy (PEEM) data has been used to show that low energy electrons ~1.35 eV could travel as far as ~15 nm in SiO_2, despite an average measured attenuation length of 1.18 nm.

VI. CONCLUSION &FUTURE SCOPE

The present 10nm and 7nm technologies are not the end. Leading manufactures keep discovering newer technologies to uphold Moore's law to their maximum possibility. Transistors less than 7nm will experience quantum tunnelling through their logic gates. Then next node is the 5mm technology. Due to the costs involved in development, 5 nm is predicted to take longer to reach market than the 2 years estimated by Moore's law. Beyond 7 nm, major technological advances would have to be made; they include vortex laser, MOSFET-BJT(Complementary Metal-Oxide Semiconductor Field Effect Transistor – Bipolar Junction Transistor) dual-mode transistor, 3D Packaging, microfluidic cooling, PMOS, Vacuum transistors, t-rays, Extreme Ultraviolet Lithography, carbon nanotube transistors, Silicon photonics, graphene, phosphorene, Organic semiconductors, Gallium arsenide, indium gallium arsenide, nano-pattening and reconfigurable chaos based microchips. All these new technologies pave way for the future in semiconductor industry. Finally the future manufacturing trends of the semiconductor industry in the upcoming years is as shown in figure 3.

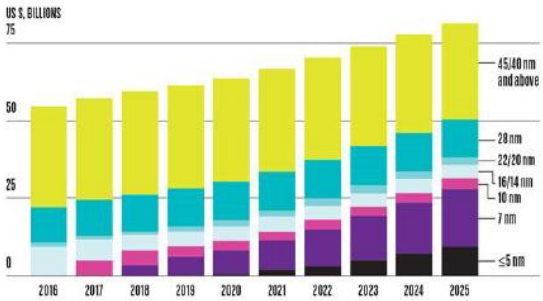

Figure 3: Future manufacturing trends

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