Adaptive Supply Voltage for Combinational circuits using MPR

1Birudu Venu, 2N. Adinarayana
1PG Student (M.Tech), Dept. Of ECE, KKR & KSR Institute of Technology & Sciences, Guntur
2Professor, Dept. Of ECE, KKR & KSR Institute of Technology & Sciences, Guntur

Abstract— VLSI circuits of the 45-nm technology and beyond are increasingly affected by process variations as well as aging effects. Overcoming the variations inevitably requires additional power expense, which in turn aggravates the power and heat problem. Adaptive supply voltage (ASV) is an arguably power efficient approach for variation resilience since it attempts to allocate power resources only to where the negative effect of variations is strong. In this paper we propose a ASV system for designs containing many timing critical paths. This system can simultaneously provide ASV at both coarse-grained and fine grained levels, and has limited power routing overhead. The dual- ASV system is compared with conventional ASV through SPICE simulations on benchmark circuits. The results indicate that the ASV system consumes significantly less power and achieves similar performance in the presence of variations. Tanner is used as a tool for the schematic implementation of the circuit under 0.25 um technology. In this paper we are implementing the design to a combinational circuit.

Keywords— Adaptive supply voltage (ASV), Power saving, clock, Asynchronous Power Saving Controller (ASPC), Maximum power regulated circuit.

I. INTRODUCTION

As Technology continues to shrink, Process variations can have a Significant Negative Impact on Yield due to the wider Spread of Performance and Power Consumption. Post-silicon Tuning allows the Adjustment of Device characteristics after a die has been Manufactured to Compensate for the Specific Deviations that Occurred on that Particular die. One of the methods Utilizes the Transistor body Effect to change Transistor Threshold Voltage by Applying an Adaptive Body Bias (ABB) to chip Devices to Modulate Performance and Power. The other method of Performing Post-Silicon Tuning is to Adjust the Supply Voltage (ASV) to trade Performance with Power, thus Achieving a similar Effect to ABB in spite of the different Physical Mechanism, Implementation Overhead and Trade-Off Curves.

Adaptive Body Bias (ABB) and Adaptive Supply Voltage (ASV) have been showed to be Effective methods for Post-Silicon tuning of Circuit Properties to Reduce Variability. While their properties have been compared on Generic Combinational Circuits or Microprocessor Circuit sub-blocks, the Advent of Multi-Core Systems is Bringing a New Application Domain fore front. Global Interconnects are Evolving to complex Communication Channels with Drivers and Receivers, in an Attempt to Mitigate the Effects of Reverse scaling and reduce power. The Characterization of the Performance Spread of these links and the Exploration of Effective and Power-Aware Compensation Techniques for them is becoming a key design Issue.

The Effectiveness of ABB and ASV in Reducing Variability has been Assessed and Compared Mainly on Combinational Logic Circuits Key Elements of Microprocessor Critical Paths and Ring Oscillators, sometimes Achieving Counterintuitive and even Conflicting Conclusions. According to the difference in Effectiveness is so small that choosing one method over the other should mainly be based on Implementation overhead claims that although the frequency and power tuning range of ABB is more limited than that of ASV, its frequency tuning range proves effective for process-dependent performance compensation. Over the last four decades the integrated circuit industry has evolved in a tremendous pace. This success has been driven by the scaling of device sizes leading to higher and higher integration capability, which have enabled more functionality and higher performance. The impressive evolution of modern high performance microprocessors have resulted in chips with over a billion transistors as well as multi-GHz clock frequencies.

As the silicon integrated circuit industry moves further into the nanometre regime, scaling of device sizes is still predicted to continue at least into the near future. However, there are a number of challenges to overcome to be able to continue the increase of integration at the same pace. Three of the major challenges are increasing power dissipation due to clocking of synchronous circuit, increasing leakage currents causing growing static power dissipation and reduced circuit robustness, and finally regulate the power in delay time due to physical limitations in the manufacturing process. This thesis presents a number of circuit techniques that aims to help in all three of the mentioned challenges. In this Paper We Propose, a ASV system for designs containing many timing critical paths. This system can simultaneously provide ASV at both coarse-grained and fine grained levels, and has limited power routing overhead. The ASV system is compared with...
conventional ASV through SPICE simulations on benchmark circuits. The results indicate that the ASV system consumes significantly less power and achieves similar performance in the presence of variations. Tanner is used as a tool for the schematic implementation of the circuit under 0.25 um technology.

II. EXISTING SYSTEM

We focus on a process variations and circuit aging in this paper. Since the former is static and the latter is a very slow change, voltage adaptation can be performed off-line either at power on or periodically. For the off-line tuning, a test pattern generator is needed. One can either employ linear feedback shift register to generate test vectors or use test vectors saved in memory. Schematic simulation results confirm the excellent matching of the traditional and proposed ASVs. Depending on how scan flip-flops are designed, it may be possible to reuse the scan portion of a design for the output latch (e.g., utilizing 3-latch or 4-latch scan flip-flop designs [Das Gupta 81, Kuppu swamy 04]).

\[\text{fig.1 Signal transitions during the guard band interval}\]

Implementation Stability Checker and Delay Generator:

Our design approach is to modify a standard latch or flip-flop by inserting a "monitoring" circuit block which detects any 'significant' shifts in delay of the combinational logic whose output is connected to the data input of that latch or flip-flop. In this paper, we focus on rising-edge-triggered flip-flop based designs however, the presented techniques are applicable for falling-edge-triggered flip-flops and latches as well. The monitoring circuit block is based on the concept of stability checking during the guard band interval by detecting signal transitions during the guard band interval, also referred to as guard band violation. Figure 1 illustrates this point.

Guard band violation at the combinational logic output means that the combinational logic input stimulus exercises one or more paths that have aged enough to creep into the guard band interval and is now very close to turning into a delay fault. Note that, the flip-flop will still continue to capture correct logic values from the combinational logic – that is the basic difference from error detection. Figure 2 shows the block diagram of a design consisting of a flip-flop with a built-in aging sensor. An aging sensor integrated inside a flip-flop has three components: a stability checker (Fig.3), a delay element to create an interval during which stability checking is performed (Fig. 4), and an output latch to store stability checking results. Details of each aging sensor component are discussed later in this section. The delay element and the output latch may be shared among multiple flip-flops for power and area savings. Depending on how scan flip-flops are designed, it may be possible to reuse the scan portion of a design for the output latch (e.g., utilizing 3-latch or 4-latch scan flip-flop designs [Das Gupta 81, Kuppu swamy 04]).

\[\text{fig.2 Built-in aging sensor with Flip Flop}\]

Stability Checker

Figure 3 shows the design of a stability checker and Fig. 5 shows the corresponding waveforms. In the beginning of a clock cycle when Clock = 1 (i.e., Clock_b = 0), PMOS transistors T1 and T5 in Fig. 3 are on (NMOS transistors T3 and T7 are off), and the stability checker output Out = 0. This is called the precharge phase of the stability checker. The delay element (Delay) in Fig. 3 (and shown in detail in Fig. 4) introduces a delay of ‘Tclk/2 – Tg’ (assuming 50% duty cycle of Clock). Here, Tg is the guard band interval (Fig. 1). This guarantees that transistors T3 and T4 (and transistors T7 and T8) are both on during the guard band interval Tg (called the evaluate phase). During the guard band interval, PMOS transistors T1 and T5 are turned off. Stability Checker output Out becomes 1 if and only if the combinational logic output OUT transitions from 1 to 0 or 0 to 1 once or multiple times during the guard band interval, i.e., the guard band is violated. The output latch in Fig. 2 is responsible for holding the state of the sensor output whenever the stability checker catches any guard band violation (i.e., stability checker output is 1). Example waveforms are shown in Fig. 5.

\[\text{fig.3 Design of a stability checker}\]

Delay Generator

Design of an aging resistant delay element is shown in Fig. 4. Since PMOS aging is a slow process, aging sensors can be turned off most of the time to ensure that they do not age significantly. This requires an additional
slow global input signal, Monitor in Fig. 4. This signal may be derived from the scan enable signal. When Monitor = 1, aging monitoring is turned on and the delay element outputs a delayed version of Clock_b. When Monitor = 0, aging monitoring is turned off and the delay element produces 1. Turning aging monitoring off also reduces power consumption of the delay element. However, we must ensure that the source-gate junctions of all PMOS transistors used in generating the guard band interval must not be forward biased when aging monitoring is turned off. The aging resistant delay element design in Fig. 3.4 accomplishes this in the following way discussed next.

When Monitor = 1, aging monitoring is turned on and the series of NAND gates (G2, G3, G4) introduce the delay required to produce a delayed version of Clock_b. When Monitor = 0, each NAND gate (G2, G3, G4) produces a 1 at its output irrespective of the other input signal. As a result, the corresponding PMOS transistor in the following NAND gate that this output is connected to is off and doesn’t age. Note that, the PMOS transistor in a NAND gate connected to the Monitor signal continues to age. However, this PMOS transistor will not affect the delay of the circuit path which produces delayed Clock_b since it is in parallel to the other PMOS transistor which is off when Monitor = 0.

To prevent aging of the first PMOS transistor connected to the clock input of the delay element, we use a NOR gate (G1) instead of NAND. The PMOS transistor inside G1 connected to the Clock input is off (and does not age) when Monitor = 0. This NOR gate inverts Clock to generate Clock_b when Monitor = 1, and produces 0 when Monitor = 0. The NOR gate output cannot be directly connected to the input of NAND gate G2 because the corresponding PMOS transistor on the circuit path producing delayed Clock_b will age when Monitor = 0. Instead, the output of G1 is connected to an inverter formed out of T11 and T13. When Monitor = 0, T10 and T12, in series with T11, are turned off ensuring that T11 does not age. When Monitor = 0, T13 is off and T14 is on producing 1 at the input of G2. This ensures that the PMOS transistor of G2 connected to the circuit path producing delayed Clock_b does not age when Monitor= 0.

Fig. 5 Transition at guard band interval

III. PROPOSED SYSTEM

We propose a ASV system to solve the problems. In this system, each selected circuit block has two power supply lines—one belongs to a global and coarse-grained ASV and the other is a local and fine-grained ASV. This system has the following two advantages.

1) A few paths of variations can be handled by the fine grained ASV and widespread variations can be taken care of by the coarse-grained ASV. Thus, this system can solve the granularity uncertainty problem.

2) The overhead of the coarse-grained ASV is no greater than the conventional ASV. With the help from the coarse-grained ASV, the fine-grained ASV can focus on a small number of gates, and therefore, allows low overhead of power and delivery network for supply voltage generation.

In a ASV system, usually one supply voltage is higher than the other. Then, which one is delivered at global (coarse grained) level? We choose to use the lower supply voltage at global level and the higher voltage at local level. The main reason is that local voltage generation is mostly obtained on chip and difficult to have high energy efficiency. If low supply voltage is applied locally, the power savings from the low supply voltage is largely cancelled by the waste in the supply voltage generation. In contrast, if high voltage is applied locally, its power waste can be overshadowed by the power savings from the global application of low voltage.

Fig. 6 Block diagram of proposed system

The proposed system is illustrated in Fig. 6. It is in the context of voltage-island-based designs [2], [3]. In the low VDD island, an additional power supply is obtained
by tapping off an intermediate voltage level Vf from VDD,H of its neighboring high VDD island. The level of Vf is somewhere between VDD,H and VDD,L. Vf is supplied only to the critical paths in the low VDD island. In a rare but possible case when the proposed ASV system is temporarily unable to find a nearby VDD,H island for tapping Vf due to dynamic voltage control of each voltage island, the proposed system can simply utilize global ASV to raise VDD,L. A delay variation prediction circuit \[2\] is employed. It can generate a warning signal if a delay variation is large and close to timing error. With the warning signal, we can efficiently use Vf to save overall power consumption as well as to minimize load to Vf so as to restrict overhead from generating Vf. Suppose Vf is designed to deliver power to totally up to N critical paths in a circuit block. When less than N critical paths flag variation warnings, these paths are switched from VDD,L to Vf. If more than N critical paths have warnings, VDD,L is raised like in conventional ASV. Therefore, we can achieve ASV at two levels: VDD,L at coarse-grained level and Vf at fine-grained level. Detailed descriptions about how we efficiently control Vf in conjunction with variation warning signals are discussed in Section V. In the experiment circuits presented in Section VI, we adjust VDD,L through coarse-grained ASV if more than 10%–15% of paths flag warning. When tap Vf from VDD,H, we use linear regulators \[3\]. Since Vf is generated locally, there is no significant overhead on power delivery. Although the energy efficiency of linear regulators can be low, the overall power overhead is small as they are applied in a restricted manner.

IV. RESULTS AND DISCUSSIONS

Reducing the supply voltage to reduce dynamic power consumption in CMOS devices, inadvertently will lead to an exponential increase in leakage power dissipation. We are exploiting this observation to turn off cache lines that are not likely to be accessed anymore. Our method is simple: if a cache line is not accessed within a fixed interval (called decay interval) we turn off its supply voltage using an adaptive supply voltage. We study the effect of cache-line decay on both power consumption and performance. We find that it is possible with cache-line decay to build larger caches that dissipate less leakage power than smaller caches while yielding equal or better performance. In this part, simulation and designed power optimization circuits are discussed in this section. In order to handle different scale of variations in an efficient manner, we proposed a ASV system This system allowed fine-grained ASV with simple regulator designs and low power routing overhead. This system included a progressive voltage enhancement scheme, which had large flexibility for accommodating different scenarios of variations. The effectiveness of this system was validated by SPICE simulations.

![Fig. 8 Top Module for the Proposed system](image)

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![Fig. 9 Combinational Circuit](image)

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![Fig. 10 Simulated output for Combinational Circuit](image)

Fig. 10 Simulated output for Combinational Circuit

The small power waste at the linear regulators is exchanged for a large power reduction at the rest of the circuits, which operate at a lower supply voltage. Overall, the power efficiency is improved compared to conventional methods. We focus on process variations and circuit aging. Since the former is static and the latter is a very slow change, voltage adaptation can be performed off-line either at power on or periodically. For the off-line tuning, a test pattern generator is needed. One can either employ linear feedback shift register to generate test vectors or use test vectors saved in memory.
The MPR circuit regulates the voltage level to 0.5 as the combinational circuit given is under decay condition. This method proves to be advantageous as few paths of variations can be handled by the fine grained ASV and widespread variations can be taken care of by the coarse-grained ASV. Thus, this system can solve the granularity uncertainty problem.

ASV can focus on a small number of gates, and therefore, allows low overhead of power and delivery network for supply voltage generation. This system has applications in various fields like continuous working circuits, age sensitivity circuits and radar applications etc.

We further look to include extended experiments to cover more complex configurations of dynamic voltage and frequency scaling over multiple voltage islands, stable reference voltage generation with band gap reference for enhancing reliability of MPR design, and further discussions on design automation approaches to incorporate the proposed dual-power system with the standard digital design process.

REFERENCES


Authors Profile:

BIRUDU VENU is pursuing his Master degree M.Tech in VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS in KKR & KSR Institute of Technology & Science. He has completed his B.Tech in ECE in BAPATLA ENGINEERING COLLEGE.

NADI NARAYANA is working as Professor and HOD in KKR & KSR Institute of Technology & Science. He has completed his Master Degree and pursuing Ph.D. His research work is aimed at Medical image processing.