



VLSI Designing of Low Power Radix4 Booths Multiplier

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Abstract- The operation of multiplication is present in several parts of a digital system or digital computer. It is extensively used in signal processing, graphics and scientific computation. With advancement in technology, various techniques have been proposed to design multipliers, with higher speed, lower power consumption and lesser area. Thus high speeds, low power compact VLSI implementations can be accomplished. These three parameters i.e. power, area and speed are always main traded off to accomplish. Multiplication involves two basic operations: the generation of partial products and their accumulation. Partial products can be reduced by using the Radix_4 modified Booth algorithm. The parallel multipliers like radix 4 modified booth multiplier do the computations using lesser adders and lesser iterative steps.

The design is proposed for implementation of Booth multiplier using VHDL. This compares the power consumption and delay of radix 2 and modified Booth multipliers. The modified Booth multiplier with ripple carry adder will have power reduction than the conventional radix 2 Booth Multiplier.

Keywords- Booth multiplier, Low power, modified booth multiplier, VHDL, partial product generation (PPG).

I. INTRODUCTION

Continuous advances of microelectronic technologies to make better use of energy encode data more effectively, transmit information more reliably etc. Many of these technologies possess low-power consumption to meet the requirements of various portable applications.

The energy efficient digital signal processing (DSP) modules are becoming increasingly important in wireless sensor networks, where from tens to thousands of battery-operated micro sensor nodes are deployed remotely and used to relay sensing data to the end-user. In these application/systems, a multiplier is a fundamental arithmetic unit and widely used in circuits.

Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore low-power multiplier design has been an important part in low- power VLSI system design [6]. Fast multipliers are essential parts of digital signal processing systems. The speed of multiplier operation is of great importance

in digital signal processing as well as in the general purpose processors today. The basic multiplication principle is two fold i.e., evaluation of partial products and accumulation of the shifted partial products.

The design of a low power high speed Booth multiplier and its implementation on reconfigurable hardware is being proposed. For arithmetic multiplication, various multiplication architectures like array multiplier, Booth multiplier, Wallace tree multiplier and Booth Wallace multiplier have been analyzed. Then it has been found that Booth Wallace multiplier is most efficient among all, giving optimum delay, power and area for multiplication. Low power modified Booth decoder and pipelining techniques have been used to reduce power and delay.

In booth multiplier the number of summands is reduced by recording the multiplier bit into groups that select multiples of multiplicand. From the basics of Booth Multiplication it can be proved that the addition/subtraction operation can be skipped if the successive bits in the multiplicand are same. To achieve high performance, the modified Booth encoding which reduces the number of partial products by a factor of two through performing the multiplier recoding has been widely adopted in parallel multipliers. The multiplication operations have the fixed-width property. That is, their input data and output results have the same bit width. For example, the $(2W - 1)$ -bit product obtained from W -bit multiplicand and W -bit multiplier is quantized to W -bits by eliminating the $(W - 1)$ least-significant bits (LSBs). In typical fixed-width multipliers, the adder cells required for the computation of the $(W - 1)$ LSBs are omitted and appropriate biases are introduced to the retained adder cells. The hardware complexity reduction and power saving can be achieved by directly removing the adder cells of standard multiplier. Due to this a huge truncation error will be introduced. To effectively reduce the truncation error, various error compensation methods, which add estimated compensation value to the carry inputs of the reserved adder cells. The error compensation value can be produced by the constant scheme or the adaptive scheme. The adaptive error compensation approaches

are developed only for fixed-width array multipliers and cannot be applied to significantly reduce the truncation error of fixed-width modified Booth multipliers directly. To overcome this problem, several error compensation approaches have been proposed to effectively reduce the truncation error of fixed-width modified Booth multipliers. To obtain better error performance with a simple error compensation circuit, Booth encoded outputs are utilized to generate the error compensation value.

II. LITERATURE REVIEW

Simran Kaur & Manu Bansal has designed FPGA implementation of Modified Booth Wallace Multiplier to make the multiplier faster & reduce the power consumption [1]. In “Parallel MAC Based on Radix-4 & Radix-8 Booth Encodings” authors has enhanced the speed of parallel MAC (multiplier & accumulator) by using a new Radix-5 Kogge stone adder [2]. The proposed MBM utilizes the carry select Adder (CSA) and 3-stage pipelining technique to improve the performance by reducing delay time [3]. In the “Vlsi Architecture of Parallel Multiplier– Accumulator Based on Radix-2 Modified Booth Algorithm” authors proposed CSA tree uses 1’s-complement-based radix-2 modified Booth’s algorithm (MBA) and has the modified array for the sign extension in order to increase the bit density of the operands [4]. In “Fixed Width Modified Booth Multiplier for High Accuracy”, the fixed-width modified Booth multipliers are proposed for high-accuracy [5]. In “Efficient Implementation Of 16-Bit Multiplier-Accumulator Using Radix-2 Modified Booth Algorithm And Spst Adder Using Verilog” The proposed radix-2 modified Booth algorithm MAC with SPST gives a factor of 5 less delay and 7% less power consumption as compared to array MAC [6]. In “Architecture of a Floating Point Register for an Experimental RISC CPU” an 8-bit RISC-CPU is designed at gate level using completely custom chip approach. CPU has an 8-bit integer unit and 16bit floating point unit [7]. Nishant Bano has proposed a design of modified Booth Multiplier for low power consumption [9]. The authors Soojin Kim and Kyeongsoon Cho in “Design of high-speed modified Booth multipliers operating at GHz ranges” has proposed the design for multiplication operation at very high speed (i.e very high frequency or in GHz range) [10]. The authors of “Low voltage Low-power VLSI Subsystems” have discussed the various low power VLSI system design issues to reduce the system power consumption [11]. Spartan-3E FPGA Starter Kit Board User Guide released in June 20, 2008 gives guidelines to use it& its versatility for the applications [14].

III. METHODOLOGY

Multipliers are important operands and utilize in high-speed low-power systems where a large amount of information is to be calculated. The modified Booth algorithm reduces the number of partial products by half. The modified Booth encoding (MBE) scheme is

known as the most efficient Booth encoding and decoding scheme. To multiply, multiplicand ‘X’ by multiplier ‘Y’ using the modified Booth algorithm. First group the multiplier bits ‘Y’ by three bits and encoding into one of {-2, -1, 0, 1, 2}. Prior to convert the multiplier, a zero is appended into the Least Significant Bit (LSB) of the multiplier. Table I shows the rules to generate the encoded signals by MBE scheme and Fig. 1 shows the corresponding logic diagram. The Booth decoder generates the partial products using the encoded signals as shown in Fig. 2.

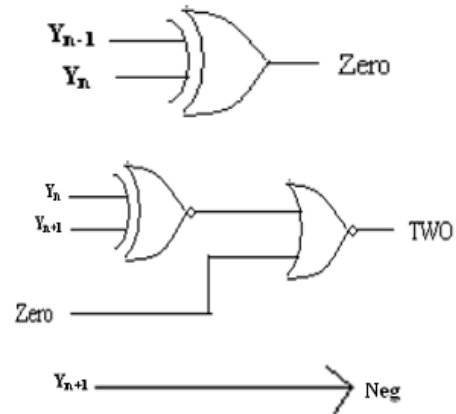


Fig 1. Booth encoder

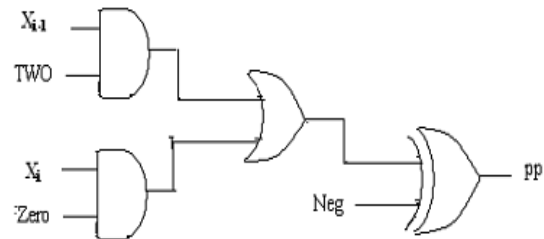


Fig 2. Booth decoder.

Table1: Truth table for modified booth encoder.

Y_{n+1}	Y_n	Y_{n-1}	Z_n	Operate	Neg	Zero	Two
0	0	0	0	0	0	0	0
0	0	1	1	$1 \times M$	0	1	0
0	1	0	1	$1 \times M$	0	1	0
0	1	1	2	$-2 \times M$	0	0	1
1	0	0	-2	$-2 \times M$	1	0	1
1	0	1	-1	$-1 \times M$	1	1	0
1	1	0	-1	$-1 \times M$	1	1	0
1	1	1	0	0	0	0	0

In an n-bit modified Booth multiplier, the number of Booth encoders is $n/2$ and the number of partial product generator (PPG) circuits is approximately n^2 , hence power consumption and die area in the Booth section is dominated by PPG. So, integration of PPG (Booth Decoder) section is more important than Booth encoder (BE) block. The conventionally used modified Booth selector computes the partial product of j^{th} bit and i^{th} row by using the equation 1.

$$PP_{ij} = (X_j \cdot X1_2 + X_j \cdot 1 \cdot X1_1) \text{ XOR Neg} \quad -(1)$$

Where X_j and X_{j-1} are the multiplicand inputs of weight 2_j and 2_{j-1} respectively, $X1_2$ and $X1_1$ determine whether the multiplicand should be doubled or not and Neg is a digit which determines if the multiplicand should be inverted or not. Booth recoding is fully parallel and carry free.

It can be applied to design a tree and array multiplier, where all the multiples are needed at once. Radix-4 Booth recoding system works perfectly for both signed and unsigned operations.

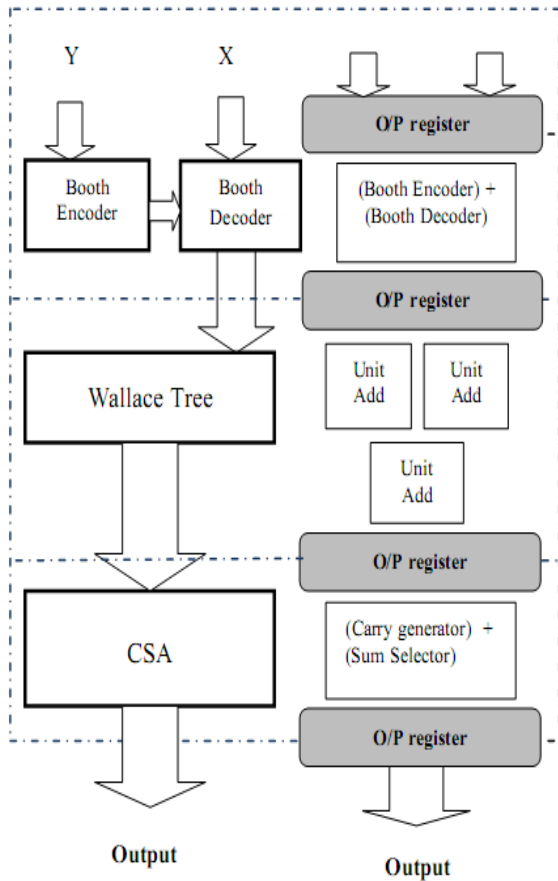


Fig 3. Block diagram of Block Diagram of Modified Booth Multiplier.

Proposed Methodology:

As it has been found that, Booth Wallace multiplier is most efficient among all, giving optimum delay, with lesser power and small chip area for multiplication. Therefore the proposed design for low power high speed Booth multiplier and its implementation on reconfigurable hardware will utilize the carry ripple adder along with the booth's algorithm to accomplish the goal.

IV. RESULT

Xilinx 8.2i ISE Simulator has been used to simulate the proposed methodology of multiplication of two 8 bit numbers using Radix-4 modified Booths algorithm. The device used by the simulator is XC3S50 of Spartan3 family with the speed of -5 which is shown in Fig. 4.

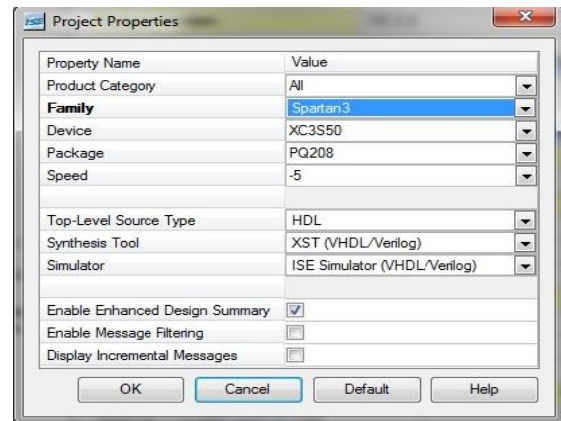


Fig. 4. Properties of Xilinx 8.2i module

The Result Can be analyze by following table,

Table 2. Multiplication of a and b

Input a[7:0]	Input b[7:0]	Output c [16:0]	Delay (ns)
92	49	4508	0
15	105	1575	500
85	124	10540	1000

The simulation result for multiplication of two 8-bit numbers is shown in the Fig. 5. Initially a=92 and b=49 with delay of 500 ns. Therefore, after 500ns the multiplication result is available in c = 4508. The power analysis of the Modified Booth's Multiplier using ripple carry adder is shown in Fig. 7. Reduction in dynamic power from 11 mW to 8.22 mW has been accomplished.

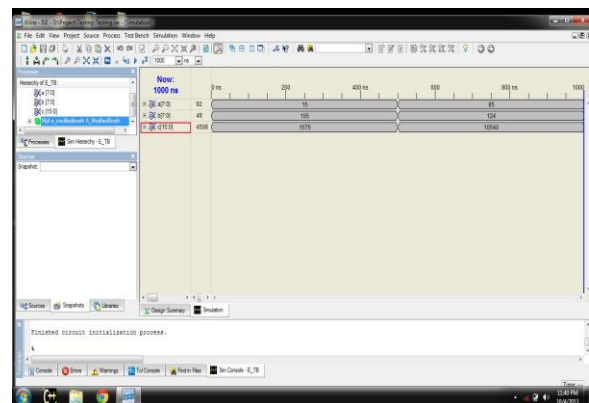


Fig. 5. Simulation results of multiplication of two 8-bit numbers.

Figure below shows the RTL schematic of the multiplier using the ripple carry adder.

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