



Design of Serial data communication using Dual Master and Slave I²C Bus Controller

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Abstract- This paper presents an experimental design and implementation of serial data communication using I²C (Inter-Integrated Circuit) multi master and multi slave bus controller using a field programmable gate array (FPGA). The I²C master bus controller was interfaced with slave. This module was designed in Verilog HDL and simulated in Modelsim 10.1c. The design was synthesized using Xilinx ISE Design Suite 14.2. I²C master initiates data transmission and in order slave responds to it. It can be used to interface low speed peripherals like motherboard, embedded system, mobile phones, set top boxes, DVD, PDA's or other electronic devices.

Keywords – Dual master, dual slave I²C, master, Modelsim, serial data communication, slave, Spartan 3AN, Xilinx.

I. INTRODUCTION

In the world of serial data communication [5], there are protocols like RS-232, RS-422, RS-485, SPI (Serial peripheral interface), Micro wire for interfacing high speed and low speed peripherals. These protocols require more pin connection in the IC(Integrated Circuit) for serial data communication to take place, as the physical size of IC have decreased over the years, we require less amount of pin connection for serial data transfer. USB/SPI/Microwire and mostly UARTS are all just one point to one point' data transfer bus systems.

They use multiplexing of the data path and forwarding of messages to service multiple devices. To overcome this problem, the I²C [1] protocol was introduced by Phillips which requires only two lines for communication with two or more chips and can control a network of device chips with just a two general purpose I/O pins whereas, other bus protocols require more pins and signals to connect devices.

In this project, we are implementing multi master and multi slave I²C bus protocol for interfacing low speed peripheral devices on FPGA It is also the best bus for the control applications, where devices may

have to be added or removed from the system. I²C protocol can also be used for communication between multiple circuit boards in equipments with or without using a shielded cable depending on the distance and speed of data transfer. I²C bus is a medium for communication where master controller [6] is used to send and receive data to and from the slave. The low speed peripheral, is interfaced with I²C master bus and synthesized on Spartan 3AN. Fig-1 shows the I²C bus system with multi master and multi slave.

When using multiple master Arbitration and clock stretching need to be considered. Arbitration decides which master is going to rule the bus.

The synopsis of the paper is as follows: In section 2, we discussed I²C protocol of our proposed design which also presents module description for our proposed system. In section 3, we present the software implementation along with algorithm and flow chart.. Finally, concluded with future scaleup in section 4.

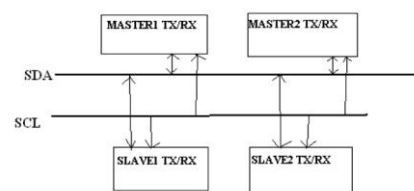


Fig-1 I/O Diagram of I²C Multi Master and Multi Slave bus controller

II. PROPOSED WORK

2.1. I²C Protocol

I²C is a two wire, bidirectional serial bus that provides effective data communication between two devices. I²C bus supports many devices and each device is recognized by its unique address.



Fig-2 (a) “START” Sequence. (b) “STOP” Sequence

The physical I²C bus consists of just two wires, called SCL and SDA. SCL is the clock line. It is used to synchronize all data transfers over the I²C bus. SDA is the data line. The SCL and SDA lines are connected to all devices on the I²C bus. As both SCL and SDA lines are "open drThe I²C bus is said to be idle when both SCL and SDA are at logic 1 level. When the master (controller) wishes to transmit data to a slave (DS1307) it begins by issuing a start sequence on the I²C bus, which is a high to low transition on the SDA line while the SCL line is high as shown in Fig- 2(a).The bus is considered to be busy after the START condition. After the START cond slave address is sent by the master. The slave device whose address matches the address that is being sent out by the master will respond with an acknowledgement bit on the SDA line by pulling the SDA line low. Data is transferred in sequences of 8 bits. The bits are placed on the SDA line starting with the MSB (Most Significant Bit). For every 8 bits transferred, the slave device receiving the data sends back an acknowledge bit, so there are actually 9 SCL clock pulses to transfer each 8 bit byte of data this is shown in Fig-3. If the receiving device sends back a low ACK bit, then it has received the data and is ready to accept another byte. If it sends back a high then it is indicating it cannot accept any further data and the master should terminate the transfer by sending a STOP sequence. In Fig-2(b) which shows the STOP sequence, where the SDA line is driven low while SCL line is high. This signals the end of the transaction with the slave device.

1.2 Serial data communication

The I²C bus has two modes of operation: master transmitter and master receiver. The I²C master bus initiates data transfer and can drive both SDA and SCL lines.[2] Slave device is addressed by the master. It can issue only data on the SDA line.

In master transmission mode, after the initiation of the START sequence, the master sends out a slave address. The address byte contains the 7 bit slave address, which is followed by the direction bit (R/ w). After receiving and decoding the address byte the device outputs

Acknowledge on the SDA line. After the slave device acknowledges the slave address + write bit, the master transmits a register address to the slave this will set the register pointer on the slave. The master will then begin transmitting each byte of data with the slave acknowledging each byte received. The master will generate a stop condition to terminate the data write.

In master receiver mode, the first byte is received and handled as in the master transmission mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the slave while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (Fig-5). The address byte is the first byte received after the start condition is generated by the master. The address byte contains the 7-bit slave address, which is followed by the direction bit (R/ w). After receiving and decoding the address byte the device inputs acknowledge on the SDA line. The slave then begins to transmit data starting with the register address pointed to by the

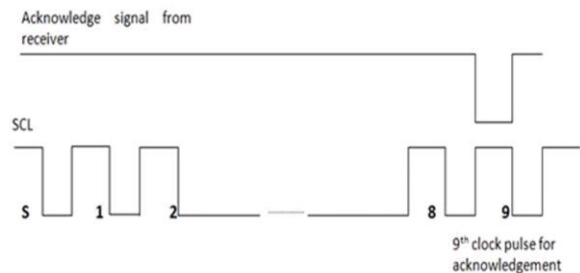


Fig-3 Acknowledgement on the I²C Bus register

Pointer. If the register pointer is not written before the initiation of a read mode, the first address that is read is the last one stored in the register pointer. The slave must receive a “not acknowledged” to end a read.

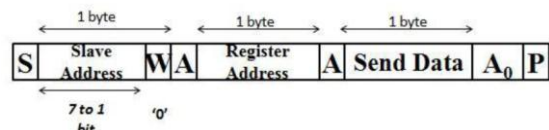


Fig -4 Master Transmission Mode

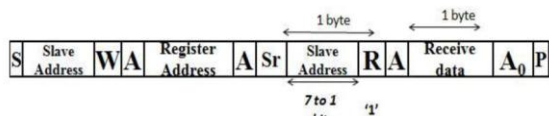


Fig- 5 Master Receiver Mode

The master transmission mode and master receiver mode is shown in above figure.

III. SOFTWARE IMPLEMENTATION

I²C bus is a medium for communication where master controller is used to send or receive data to and from slave and it is developed by Philips.

I²C master controller is designed using Verilog HDL [3] based on Finite State Machine (FSM) [8]. FSM is a sequential circuit that uses a finite number of states to keep track of its history of operations, and based on history of operation and current input, determines the next state. There are several states in obtaining the result.

Algorithm

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