Performance of Backtracking and Retracting in NOC

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Abstract - In the traffic offered by the on chip components, providing guaranteeing throughput or quality of service is the one of the most difficult tasks in network on chip design. For integrating numerous components on chip, NOC is adopted. It enables large number of computational and storage block to integrate on a single chip. Topology in NOC play important role to provide QoS. In this paper, we calculate the minimum period and frequency when 8 bit data is sent from source to destination and compare the performance between backtracking and retracting in NOC.

Index Terms:- Backtracking scheme, Network on chip, Retracting scheme, System on chip.

I. INTRODUCTION

System on chip (SOC) is an integrated circuit that integrates all components into a single chip. NOC is the only solution in SOC architecture. Some feature of SOC such as low scalability (1), complex design due to increasing number of transistor (2), non reusability (3), challenge the designer. Communication between processing elements was based on busses. The idea of networks on chip, which consists of a set of routers interconnected by link has evolved (4) and overcome the disadvantages of SOC. There are number of topology available such as mesh, torus, ring, star etc in NOC architecture. We can say network topology determine the shape of the network. Network topology determines how different nodes in a network are connected and how they communicate. The architecture of an on chip router is determine by the selection of switching methodology and may also determine service that can be provided by the network.

A. Packet switching

Packet switching and circuit switching are some basis switching method. Packet switching method is also known as store and forward switching. In packet switching data messages is divided into a number of packets and forwarded into the next router. This packet switching method has been used in many parallel computers.

B. Circuit switching

In a connection oriented communication protocol, the circuit switching method is commonly used. By established connection and reserving some communication resources the circuit switching method is performed. When a virtual circuit from a source to a destination node has been configured, and the successful connection has been informed by the destination node by sending a response packet to the source node then the message can be transmitted through the network in a pipeline manner. A control packet is sent to the network to terminate the connection circuit.

In this paper, we calculate the minimum period and frequency when 8 bit data is sent from source to destination and compare the performance between backtracking and retracting in NOC. This paper arranged as section II present literature survey, section III present network topology, section IV switch architecture, section V present backtracking and retracting, VI result and performance, section VII present conclusion and future work and finally references.

II. LITERATURE SURVEY

Sonal S. Bhople, M.A. Gaikwad, “A Comparative study of different topologies for network on chip architecture” (5). In this paper, different topologies like mesh, torus, ring, etc are compared and give the average network delay for each topology. This paper only gives comparative study of delay parameter of different topologies in network on chip architecture.

M.Mirza-Aghatabar, S.Koohi, S.Hessabi, M.Pedram “An empirical investigation of mesh and torus NOC topologies under different routing algorithm and traffic model” (6). In this paper they compare two popular NoC topologies, i.e., mesh and torus, in terms of parameter i.e power consumption, latency, and power/throughput ratio under different routing algorithms and two common traffic models, uniform and hotspot. To the best of our knowledge, this is the first effort in comparing mesh and torus topologies.
under different routing algorithms and traffic models with respect to their performance and power consumption. Torus always has better latency than mesh topology.

J. Xu, W. Wolf, and W. Zhang, “Double-data-rate, wave-pipelined interconnect for asynchronous NoCs,” (7). In this paper they mention that this new interconnect yields higher throughput, suffer less from crosstalk noise, consume less power and requires less area than traditional interconnect structures. It advantages stem from techniques including double data rate transmission misaligned repeaters, wave pipelining and clock gating.

D. Wiklund and L. Dake, “SoCBUS: Switched network on chip for hard real time embedded systems,” (8). In this paper, SOCBUS has introduced and analyzed the operational principle of this SOCBUS. They mention that the system is not suitable for general purpose computation platforms because high probability of route blocking occurs when running without schedule. Limiting the distance of communication in random pattern is important; it will allow higher bandwidth usage without saturation.

L. Zhang, Y. Hu, and C. C.-P. Chen, “Wave-pipelined on-chip global interconnects,” (9). In this paper they compared flip flop pipelining (FFP) and wave pipelining. Wave pipelining presents 18% better performance than FFP. Flip flop pipelining performs better in short interconnects while wave pipelining is better for long interconnects.

P. T. Wolkotte, G. J. M. Smit, G. K. Rauwerda, and L. T. Smit, “An energy-efficient reconfigurable circuit-switched network-on-chip,” (10). In this paper for a NOC they proposed a new reconfigurable circuit-switched router. They compare circuit switch router and packet switch router in terms of power consumption, size and throughput. The circuit switch router has smaller chip size, lower power consumption and higher maximum throughput.

Partha Pratim Pande, Michael Jones Cristian Grecu, André Ivanov, Resve A. Saleh, “Performance Evaluation and Design Trade-Offs for Network-on-Chip Interconnect Architectures,” (11). In this paper they focused on performance evaluation of a set of recently proposed NOC architectures with realistic traffic models, using a deterministic routing without addressing the effect of different routing algorithms.

L. Benini and G. De Micheli, “Networks on chips: A new SoC paradigm,” (12). In this paper they gave idea why network-on-chip being adopted in system on chip. Mentioning network on chip is being adopted as a scalable communication-centric solution for integrating numerous on chip components i.e. processing element, sub blocks, and intellectual properties (IPs). On-chip micronetworks designed with a layered methodology; meet the distinctive challenges of providing functionally correct, reliable operation of interacting system-on-chip components.

In this paper, we compare the performance between backtracking and retracting in NOC.

III. NETWORK TOPOLOGY

Network topology is the arrangement of the various elements that is link, node etc. It refers to the shape of the network. Network topology determines how different nodes in a network are connected and how they communicate. There are many network topology in NOC architecture such as mesh torus, ring, tree star etc. Mesh based network topology is one of the most commonly used on chip network topology. In mesh topology, the implementation of routing function is simpler and can be characterized well. The mesh architecture is widely used and preferable in network architecture. There are two types in mesh topology i.e. full mesh topology and partial mesh topology For 2-D mesh topology, the number of communication channel is \( L_{\text{mesh}} = 2N(M-1) \), where \( N \) is the number switch in row and \( M \) is the number of switch in column. The switch under mesh topology in NOC can take limited number of link between switch.

![Fig 1: (a) Ring topology, (b) Star topology, (c) Mesh topology, (d) Torus topology, (e) Bus topology, and (f) Tree topology.](image-url)

The most important and mesh like topology is torus topology. The additional communication links is the main difference between mesh and torus topology. A node at the edge of the network is connecting with
another node at the opposite edge in the same horizontal or vertical path. In 2-D torus, the total number of communication channel is given as \( L_{TORUS} = 2NM \), where \( N \) is the number switch in row and \( M \) is the number of switch in column. In ring topology each node connects too exactly to other nodes, forming one continuous pathway for signals through each node - a ring. Data travels from node to node, with each node along the way handling every packet. Ring networks may be disrupted by the failure of any single link. A node failure or cable break might isolate every node attached to the ring. It performs better than a bus topology under heavy network load and makes it easy to identify and isolate faults. Bus topology is the simplest topology. All nodes are connected to the single cable or bus, by the help of interface connector. In Star topology, a central device called hub connected all components of network. All the data on the star topology passes through the central device before reaching the intended destination. As compared to bus topology it gives better performance. Centralized management helps in monitoring the network. But, too much dependency on central device has its own drawback. Tree topology is the extension of bus and star topologies. In tree topology expansion of network is possible, error detection and correction is easy. If a segment is damaged, other segment are not affected. But the maintenance become difficult if more and more nodes and segment are added.

IV. SWITCH ARCHITECTURE

The switch architecture has the two main components. They are control path and data path. The data path is CROSSBAR with internal transceivers to support a direct-forwarding of the source-synchronous data. The CROSSBAR has two functions direct-forwarding pipelined data in the transmission phase and providing connection for probe headers in the setup phase under the control of Ctrl Outs. The control part includes Ctrl In, Ctrl Out, and arbiter.

![Switch Architecture](image)

Processing the incoming probe headers from the wrapper or upstream switches is in charge by ctrl In, after monitoring the output status and make request to arbiter to grant it access to the desires ctrl out. In a switch there are five bidirectional ports, four are connected to corresponding neighboring ports, and the remaining port is connected through a wrapper to the on chip IP.

A. End to End flow control operation

Path is use to link source and destination if the path is block the data wait till the block path becomes free. Due to this the path delay degraded the performance. It is important to search an alternative path, instead of waiting for busy link to become idle. In backtracking the probe header will search for alternative link, instead of waiting for busy link to become idle. But, in without backtracking instead of searching alternative path they wait till the path becomes free.

![End to End Flow Control Operation](image)

V. BACKTRACKING AND RETRACTING

The switch is arranged in 8 x 8 matrix form. Switch 0 is the source and switch 12 is the destination and the original set up link is 0—1—2—3—4—12. Data is sending from source to destination.

![Switch in 8x8 Mesh Structure](image)

With backtracking path set up: (s) 0—1—2—3—11—12. But in retracting path set up: (s) 0—1—2—3—2—1—0 (facing link block), and so on. This requires many hops. Thus retracting path set need until link between switches 3 and 4 becomes free.

VII. RESULT AND PERFORMANCE
The simulation of MUX based crossbar structure is done using Modelsim6.2f. The synthesis is carried out using Xilinx 10.1. The 8 bits data is sent from source to destination i.e. switch 0 to switch 12.

In backtracking when sending 8 bits data from switch 0 to 12 (using Xilinx 10.1 with FPGA 3AN) the minimum period is 4.05 ns and the max freq is 246.91 MHz, and when sending 8 bit data from switch 0 to 63 (8x8) the minimum period is 7.738 ns and the maximum frequency is 129.232 MHz. In retracting scheme the period is more and the frequency is less due to waiting the link to become free. This backtracking scheme save time and increase the performance of the NOC.

Table 1: - Backtracking scheme output

<table>
<thead>
<tr>
<th>Switch size</th>
<th>Source</th>
<th>Destination</th>
<th>Period</th>
<th>Max freq</th>
</tr>
</thead>
<tbody>
<tr>
<td>8x8</td>
<td>0</td>
<td>12</td>
<td>4.05ns</td>
<td>246.91 MHz</td>
</tr>
<tr>
<td>8x8</td>
<td>0</td>
<td>63</td>
<td>7.738ns</td>
<td>129.232 MHz</td>
</tr>
</tbody>
</table>

VII. CONCLUSION AND FUTURE WORK

The Switch structure is designed and simulation is done. It is important to search an alternative path, instead of waiting for busy link to become idle. In backtracking the probe header will search for alternative link, instead of waiting for busy link to become idle. But, in retracting instead of searching alternative path they wait till the path becomes free. Backtracking provide better performance than retracting. In future, we can synthesis and implement using torus topology and can compare the period/latency and performance of backtracking.

VIII. REFERENCES


