



Design Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme.

¹M.Greeshma, ²P.Hareesh

E.C.E Department, Sir C.R.Reddy college of Engg, Andhra University
Email: ¹mrsygreeshma2@gmail.com, ²hareeshpancheti@gmail.com

Abstract— In this paper, analysis of average power, delay and power delay product is done by shift register (PIPO) using 90nm technology. Low power flip-flops are crucial for the design of low-power digital systems. As Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices are scaled down to nanometer ranges, Complementary MOS (CMOS) circuit's total Power consumption has a new definition. Due to integration of millions of components and shrinking process technology, nowadays leakage power tends to play a major role in total power consumption. In this paper, the shift registers are designed using 90nm technology with 1GHz frequencies and their performance are analyzed.

Index Terms—Flip-flop (FF), low power, pulse-triggered.

I. INTRODUCTION

Flip-Flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. The digital designs nowadays often adopt intensive pipelining techniques and employ many FF rich modules and also estimated that the power consumption of clock system, which consists of clock distribution networks and storage elements is as high as 20% to 45% of the total system power. Pulse triggered flip flop (P-FF) is considered as a popular alternative to the conventional master slave based FF in the application of high speed operations. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master slave configuration, and is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less sensitive to clock jitter. The pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network. Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit. In an

implicit type P-FF, the pulse generator is a built in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the discharging path while the latter needs to physically generate a pulse train. Implicit-type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low power techniques such as conditional capture, conditional precharge, conditional discharge, or conditional data mapping are applied.

II. PROPOSED P-FF DESIGN BASED ON A SIGNAL FEED THROUGH SCHEME

A. Conventional Explicit Type P-FF Designs P-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate. Without generating pulse signals explicitly, implicit type P-FFs are in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an n-bit register). In this brief, we will thus focus on the explicit type P-FF designs only.

To provide a comparison, some existing P-FF designs are reviewed first. Fig. 1(a) shows a classic explicit P-FF design, named data-closeto-output (ep-DCO). It contains a NAND-logic-based pulse generator and a semidynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node X. The pulse width is determined by the delay of three inverters.

This design suffers from a serious drawback, i.e., the internal node X is discharged on every rising edge of the clock in spite of the presence of a static input “1.” This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed . Fig. 1(b) shows a conditional discharged (CD) technique .

An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains “1.” In addition, the keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up pMOS transistor only. Fig. 1(c) shows a similar P-FF design (SCDFF) using a static conditional discharge technique . It differs from the CDFF design in using a static latch structure. Node X is thus exempted from periodical precharges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. The modified hybrid latch flipflop (MHLFF) shown in Fig. 1(d) also uses a static latch. The keeper logic at node X is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node X when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node X is not precharged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT) is applied to the discharging transistor MN3. Second, node X becomes floating in certain cases and its value may drift causing extra dc power . A TSPCFF a signal feed-through technique to improve this delay. Similar to the SCDFF design, the TSPCFF design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node X . Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme) as shown in fig (e).

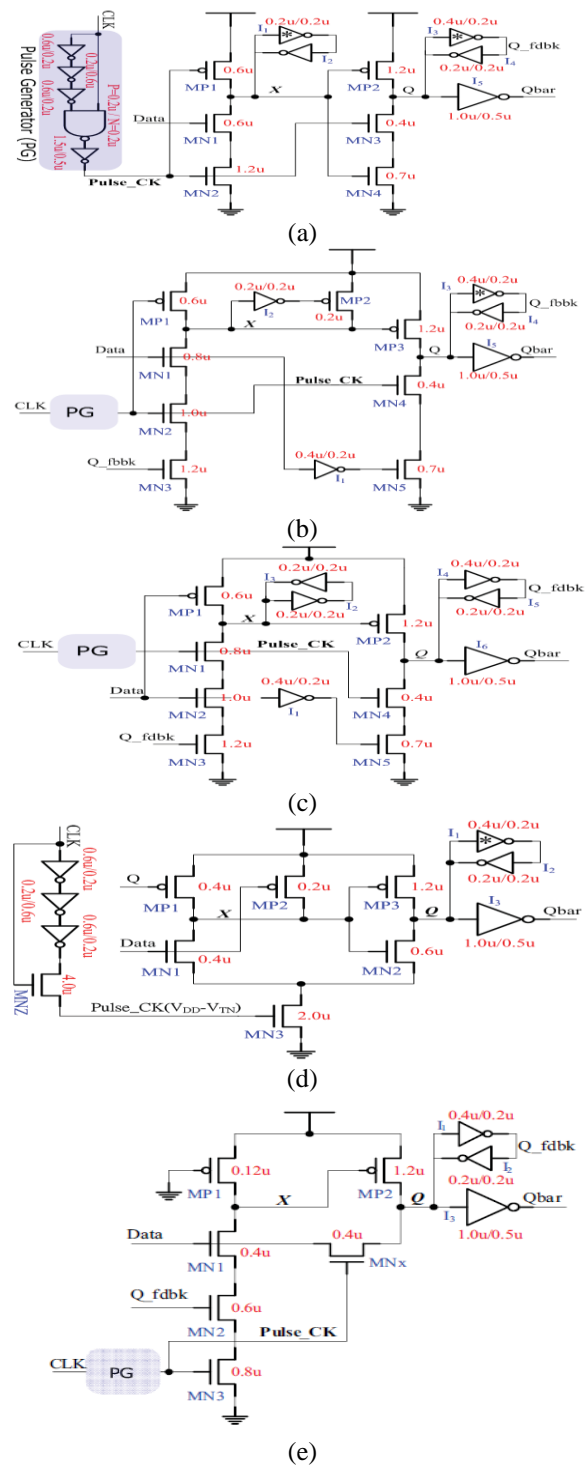


Fig. 1. Conventional P-FF designs. (a) ep-DCO . (b) CDFF .(c) Static-CDFF . (d) MHLFF.(e) TSPCFF

B. Proposed P-FF Design Our Proposed Low power Clocked Pass Transistor Flip-Flop Design by using the Pass Transistor Logic family idea we are designing this circuit as well as by using the pass transistor logic we are using only one clocking transistor so it will be Consuming only less power in the clock network of the Flip flop when compared to all other circuits. In this design reduced the discharging path X, avoids unnecessary internal node transitions to reduce power consumption and delay. This circuit X node

discharging N1&N2 transistor only. So we will be having much reduced power and area when compared to the other two designs. At the same time due to the reduced no of transistor count we can reduce the delay oriented things also. Thus we are reducing the overall switching delay and power, area consumption. So this circuit will be acting as good sequential elements when compared to other flip-flop design.

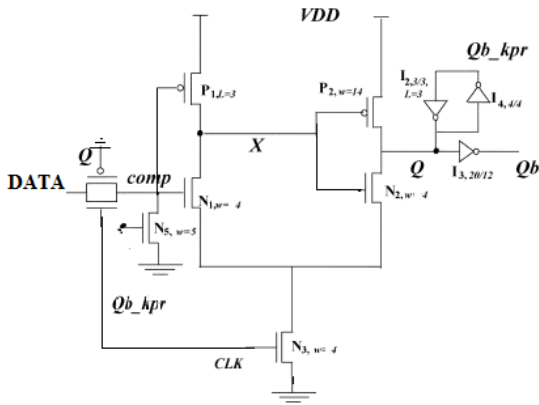


Fig. 2. Schematic of the proposed P-FF design.

III. SHIFT REGISTERS

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All flip-flop is driven by a common clock. There are different kinds of shift registers.

- * Serial in serial out shift register.
- * Serial in parallel out shift register.
- * Parallel in parallel out shift register.
- * Parallel in serial out shift register.

The storage capacity of a register is the

Total number of bits (1 or 0) of digital data it can retain. Each stage (flip flop) in a shift register represents one bit of storage capacity. Therefore the number of stages in a register determines its storage capacity.

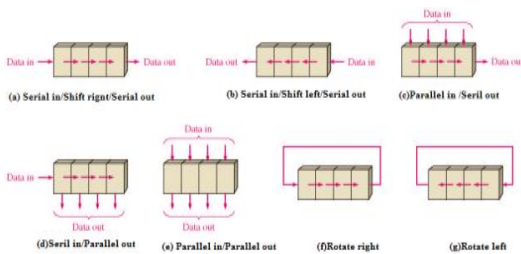


Figure 3(a): Basic data movement in shift registers .

Parallel in Parallel out Shift Register:

For parallel in parallel out shift registers, all data bits appear on the parallel outputs immediately following

the simultaneous entry of the data bits. The following circuit is a four-bit parallel in parallel out shift register constructed by d flip-flops and shown in fig 1.1(a).(b)(c).

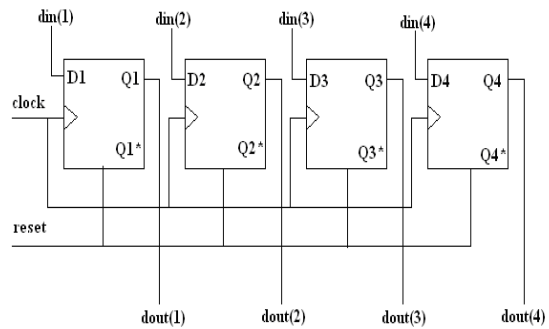


Figure 3(b): Parallel in Parallel out Shift Register.

IV. SIMULATION RESULTS

To evaluate the performance, shift registers discussed in this paper are designed using 90-nm CMOS technology. All simulations are carried out using MICROWIND simulation tool at nominal using MICROWIND simulation tool at nominal conditions with 1GHz frequency range. flip-flop based Parallel in Parallel out Shift Register layout design in Soft Ware Microwind tool is shown in Fig. 4(a) & 4(b).The layout simulation window appears with inputs and output as shown in Fig.4(c) 4(d),the power consumption is also shown on the right bottom portion of the window.

Parallel in Parallel out Shift Register:

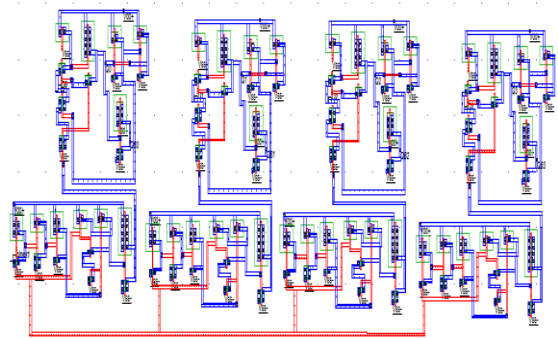


Figure 4(a) Parallel in Parallel out Shift Register using TSPCCF in Soft Ware Microwind tool

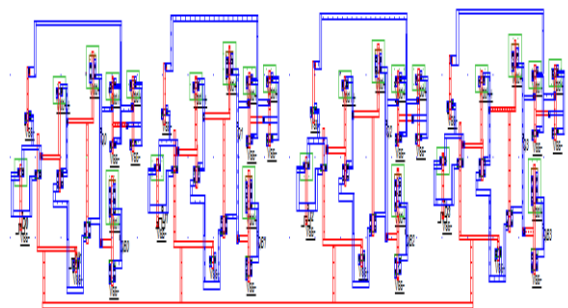


Figure 4(b) Parallel in Parallel out Shift Register using Proposed PFF in Soft Ware Microwind tool.

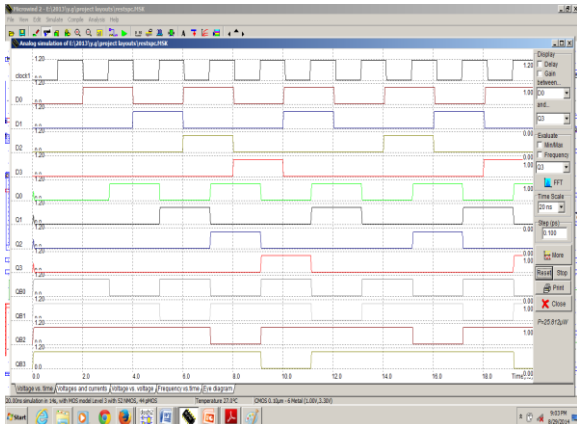


Figure 4(c) Power consumed by Parallel in Parallel out Shift Register using TSPCFF

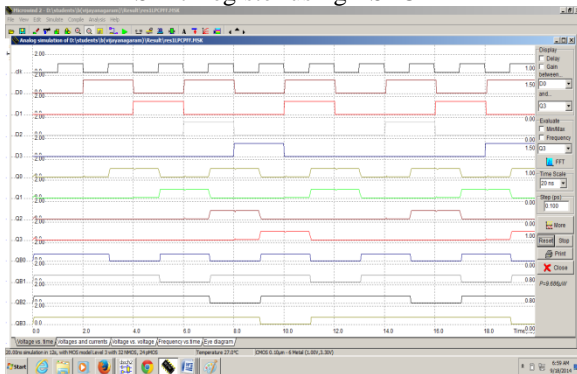


Figure 4(d) Power consumed by Parallel in Parallel out Shift Register using Proposed PFF

Table 1. : Comparison of various Parallel in Parallel out Shift Register designs.

Parameters	PIPO Shift register using EP-DCO	PIPO Shift register using SCD FF	PIPO Shift Register using CDF F	PIPO Shift Register using MHL FF	PIPO Shift Register using TSPC FF	PIPO Shift Register using PTLF FF
No. of transistors	112	124	120	76	96	56
Area μm^2 UMC CMOS-90nm	699.6	796.9	753.7	607.6	728.2	461.6
Average Power(μW) using UMC CMOS-90nm Technology. (μW)	31.2	30	29	26.8	25.8	9.46



V. CONCLUSION

This paper concludes that PTLF Flip-Flop designed with 14 Transistors is having less power consumption. The Flip-Flops are simulated for 50nm technology using the MICROWIND Tool. The comparisons of 3 Parallel in Parallel out Shift Register are shown in Table 1 to verify the designed methods using UMC CMOS 90-nm technology. With all these results Parallel in Parallel out Shift Register using PTLF speed performance and power are better than Ep-DCO, MHLFF, CDFF, SCDF, TSPCFF P-FF designs.

REFERENCES

- [1] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 807–811, May 1998.
- [2] K. Chen, "A 77% energy saving 22-transistor single phase clocking Dflip-flop with adoptive-coupling configuration in 40 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Nov. 2011, pp. 338–339.
- [3] E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, "Conditional pushpull pulsed latch with 726 fJops energy delay product in 65 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 482–483.
- [4] H. Partovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 1996, pp. 138–139.
- [5] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R. Wang, A. Mehta, R. Heald, and G. Yee, "A new family of semi-dynamic and dynamic flip-flops with embedded logic for high-performance processors," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 712–716, May 1999.
- [6] V. Stojanovic and V. Oklobdzija, "Comparative analysis of masterslave latches and flip-flops for high-performance and low-power systems," *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 536–548, Apr. 1999.