Graphene Based Transistor: G-FET

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Abstract— It has come to a time, when the search beyond silicon for using it in transistors has gained serious importance. If Gordon Moore's prediction is to be substantiated in today's world, then a post silicon age in the semiconductor industry is to be ushered soon. In this scenario, graphene-derived nanomaterials are emerging as promising candidates for post-silicon electronics devices. This paper focuses on demonstrating and studying field effect behaviour in graphene and graphite-based devices. It also provides an introduction to the theoretical aspects of graphene and then reviews the properties of graphene that are relevant to electronic devices and examine their effects on the performance of graphene based transistors in both logic and radiofrequency applications. One may conclude that the excellent mobility of graphene may not, as is often assumed, be its most compelling feature from a device perspective. Rather, it may be the possibility of making devices with channels that are extremely thin that will allow graphene field-effect transistors to be scaled to shorter channel lengths and higher speeds without encountering the adverse short-channel effects that restrict the performance of existing devices.

Keywords— Ambipolar, CMOS, confocal, field-effect transistor (FET), graphene, MOSFET, quasi-ballistic, spin coating, transistor.

I. INTRODUCTION

Every now and again, a single paper ignites a revolution in science and technology. Such a revolution was started in October 2004, when condensed-matter physicists reported that they had prepared graphene two dimensional sheets of carbon atoms—and observed the electric field effect in their samples.

An example of the expectancy for novel materials can be found in the semiconductor industry where new forms of carbon have been vying to substitute silicon. The International Technology Roadmap for Semiconductors (ITRS), which is sponsored by the world's top chip manufacturing companies, has forecasted the end of CMOS-based technology by the year 2022.

ITRS has the objective of ensuring cost efficient advancements in IC manufacturing, and thus the reasons for the CMOS demise is both economical and practical. Silicon has the physical limitation of not being able to exist below 10 nm as a crystalline solid, as the thermal fluctuations due to the generated heat (in micro circuitry) in that range makes it turn amorphous. The continually downsizing channel widths in modern circuitry, thus has a dead end in less than a decade. To

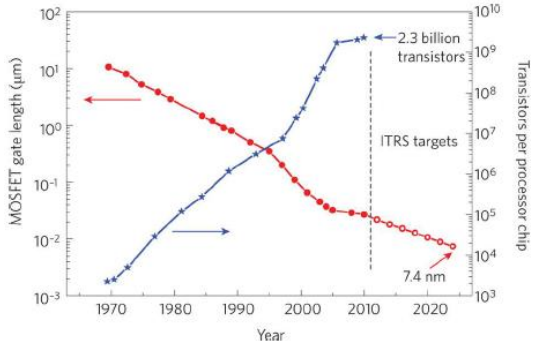


Fig.1. Evolution of MOSFET gate length & ITRS (filled and open red circles resp.), and number of transistors per processor chip (blue stars).

continue the advancements in this field, one must indulge in a suitable substitute. Carbon has been widely tipped as this substitute. The reason for the candidature is its impressive allotropes, and its similarity with silicon on the VI-A column on the periodic table. Interestingly, silicon's predecessor, germanium also hails from the same column. Although, both silicon and carbon have the same number of electrons in the outermost electronic shell, and hence similar chemical properties, the size of the electronic wave functions and their energy vary significantly. (This difference can be seen in the Coulomb interactions of the respective electron systems. Silicon's larger electron cloud shields these interactions amongst its electrons.) Carbon also has the highest melting of all elements, around 3500^0C (while silicon melts at 1700^0C). Considering these properties, swapping silicon for one of carbon's allotropes seems a logical choice, so the research community has been searching for an ideal allotrope which matches the needs. In the recent past, two carbon allotropes had become prominent contenders to replace silicon - nanotubes and graphene. Graphene is a two-dimensional honeycomb lattice of carbon rings just one atom thick, while nanotubes can be considered as rolled-up graphene sheets. They both have equally impressive mechanical and electronic properties. Carbon nanotubes (CNTs) had dominated research news in the 90's with

their widespread potential in various fields of applications ranging from medicine to electronics. However, they have been facing unresolved challenges involving their controlled growth with desired chirality, purity and dispersion. In the electronic world, in spite of their first claim to fame - charge carrier mobility of more than 100,000 cm2/Vs at room temperature - the unpredictability of their electronic nature (metallic or semiconducting) on production, has dented their chances of replacing silicon. Though younger, graphene has leapfrogged nanotubes in this scene, primarily due to the seemingly simpler methods of production and consistent electronic behaviour (semi-metallic) which can be modified according to use. Graphene's charge carrier mobilities are measured to be over 200,000 cm^2/Vs at room temperature. But unlike CNTs, which require a different set of processing techniques from silicon, graphene shares a similar set of processing techniques currently used for silicon. Graphene is also the thinnest known material, which enables it to be transparent, thereby providing an attractive offer for the usage in optoelectronic devices like photovoltaics. The competition between the two allotropes is gradually also extending to other fields like chemical and bio-sensors, mechanical resonators etc. But to go from lab scale to mass scale, engineers still need to devise methods to make industrial quantities of large, uniform sheets of pure, single planed graphene. This thesis concentrates on the electronic properties of graphene and elucidates its stance in post-silicon electronics (or nano-electronics due to the current dimensions of operation) from a material point of view. It investigates prototype field effect transistors (FETs) with graphene as conducting channel. This work aims to study this material's electronic properties for potential applications, as there are some pertinent challenges remaining about graphene, including its low (intrinsic) on-off ratios, voltage gain, substrate effects and scalability.

II. THEORY

1. Basic Structure of Graphene:

Graphene is a two-dimensional sheet of sp^2 bonded carbon atoms (Figure 2.1) arranged in a honeycomb crystal structure with two carbon atoms in each unit cell. Thermodynamically stable graphene sheet was experimentally discovered in 2004 by Giem and Novoselov. Sp^2 hybrids of each carbon atom contribute to form σ bonds with three other carbon atoms in trigonal planar structure of graphene. These σ bonds with the length of 1.42 Å are responsible for mechanical properties of graphene. The p orbitals of adjacent carbon atoms are normal to the planar structure, and can bind to form a half-filled π band which gives rise to graphene's unique electronic properties.

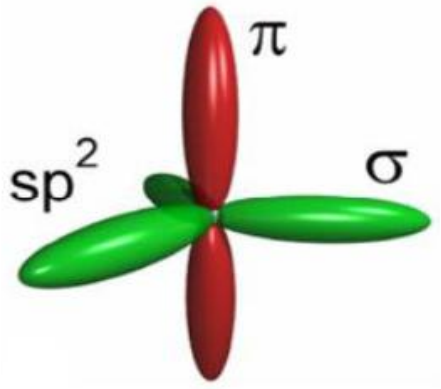


Figure 2.1: sp^2 and p orbitals of carbon atoms in graphene.

Graphene's lattice structure can be considered as two equivalent triangular sub-lattices A and B with inversion symmetry (Fig. 2.2a). The corresponding energy bands of these two sub-lattices intersect at zero energy at K points, called Dirac points, of reciprocal lattice (Fig. 2.2b and 2.2c). The dispersion relation near Dirac points is linear, and has no band gap. Thus, graphene is considered as a zero band gap semiconductor or a semimetal in which Dirac Equation governs the charge carrier behaviour near Dirac points at low energies.

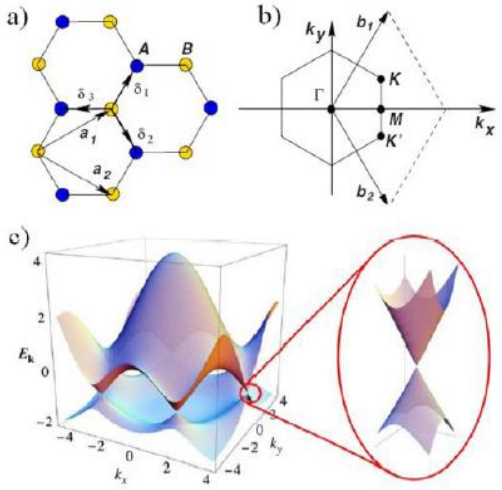


Figure 2.2: a) Lattice structure of graphene consists of two trigonal lattices A and B. b) First Brillouin zone of graphene lattice. c) Dispersion relation of graphene in fist Brillouin zone.

Graphene's linear dispersion relation at low energies near the six Dirac points can be described by equation, leading to zero effective mass for electrons and holes which move with a constant speed called Fermi velocity.

$$E = \pm \hbar \vartheta_f \sqrt{k_x^2 + k_y^2}$$

where ϑf (≈106 m/s) is the Fermi velocity of electron and holes in graphene. So, considering linear dispersion relation in graphene, charge carriers are regarded as Massless Dirac Fermions in analogy to relativistic massless particles like phonons.

2. Fundamental Characteristics of graphene:

Earlier, it was theoretically believed that two dimensional compounds could not exist due to thermal instability when separated. After studying suspended graphene sheets by transmission electron microscopy it was found that the reason for the 2-D structure was due to the slight rippling in the graphene, modifying the structure of the material. Later on, a more conclusive research suggested that it is actually due to the fact that the carbon to carbon bonds in graphene are so small and strong that they prevent thermal fluctuations from destabilizing it.

2.1) Electronic Properties: One of the most useful properties of graphene is that it is a zero-overlap semimetal (with both holes and electrons as charge carriers) with very high electrical conductivity. Carbon atoms have a total of 6 electrons; 2 in the inner shell and 4 in the outer shell. The 4 outer shell electrons in an individual carbon atom are available for chemical bonding, but in graphene, each atom is connected to 3 other carbon atoms on the two dimensional plane, leaving 1 electron freely available in the third dimension for electronic conduction. These highly-mobile electrons are called pi (π) electrons and are located above and below the graphene sheet. These pi orbitals overlap and help to enhance the carbon to carbon bonds in graphene. Fundamentally, the electronic properties of graphene are dictated by the bonding and anti-bonding (the valance and conduction bands) of these pi orbitals.

Combined research over the last 50 years has proved that at the Dirac point in graphene, electrons and holes have zero effective mass. This occurs because the energy – movement relation (the spectrum for excitations) is linear for low energies near the 6 individual corners of the Brillouin zone. These electrons and holes are known as Dirac fermions, or Graphinos, and the 6 corners of the Brillouin zone are known as the Dirac points. Due to the zero density of states at the Dirac points, electronic conductivity is actually quite low. However, the Fermi level can be changed by doping (with electrons or holes) to create a material that is potentially better at conducting electricity than well-known conductors such as copper at room temperature.

Tests have shown that the electronic mobility of graphene is very high, with previously reported results above 15,000 cm^2/Vs and theoretically potential limits of 200,000 cm^2/Vs (limited by the scattering of graphene's acoustic photons). It is said that graphene electrons act very much like photons in their mobility due to their lack of mass. These charge carriers are able to travel sub-micrometer distances without scattering; a phenomenon known as ballistic transport. However, the quality of the graphene and the substrate that is used will be the limiting factors. With silicon dioxide as the substrate, for example, mobility is potentially limited to 40,000 cm^2/Vs.

2.2) Mechanical Strength: Another of graphene's stand-out properties is its inherent strength. Due to the strength of its 0.142 Nm-long carbon bonds, graphene is the strongest material ever discovered, with an ultimate tensile strength of 130,000,000,000 Pascals (or 130 Giga Pascals), compared to 400,000,000 for A36 structural steel, or 375,700,000 for Aramid (Kevlar). Not only is graphene extraordinarily strong, it is also very light at 0.77milligrams per square meter (for comparison purposes, 1 square meter of paper is roughly 1000 times heavier). It is often said that a single sheet of graphene (being only 1 atom thick), sufficient in size enough to cover a whole football field, would weigh under 1 single gram.

What makes this particularly special is that graphene also contains elastic properties, being able to retain its initial size after strain. In 2007, Atomic force microscopic (AFM) tests were carried out on graphene sheets that were suspended over silicone dioxide cavities. These tests showed that graphene sheets (with thicknesses of between 2 and 8 Nm) had spring constants in the region of 1-5 N/m and a Young's modulus (different to that of three-dimensional graphite) of 0.5 TPa. Again, these superlative figures are based on theoretical prospects using graphene that is unflawed containing no imperfections whatsoever and currently very expensive and difficult to artificially reproduce, though production techniques are steadily improving, ultimately reducing costs and complexity.

3. Other properties of Graphene

Graphene's non-electronic properties are very impressive. Graphene displays a room-temperature thermal conductivity of 5000 W/mK, and the unique property of expanding on decreasing the temperature. Graphene is also found to be impermeable to gases and can be useful for sensing applications.

Graphene's ability to absorb a rather large 2.3% of white light is also a unique and interesting property, especially considering that it is only 1 atom thick. This is due to its aforementioned electronic properties. Adding another layer of graphene increases the amount of white light absorbed by approximately the same value (2.3%).

4. Graphene production methods

In the early work of Novoselov et al., isolated graphene sheet was produced via mechanical exfoliation which is the micromechanical cleavage of graphite. Although mechanical exfoliation is suitable for laboratory research purposes, resulted micron size graphene flakes cannot be easily scaled up for mass production. The methods developed for large scale graphene production are epitaxial growth from single-crystal silicon carbide substrates, chemical vapour deposition techniques, and self-assembly of soluble graphene.

4.1) Mechanical Exfoliation: Graphite is made of sheets of graphene kept together by Van Der Waals force. As a result, graphite can be exfoliated with a "Scotch Tape", and continuation of the peeling process can lead to multilayer and even single-layer graphene as it was done for its discovery.

Next, the graphene flakes are transferred onto a suitable substrate such as silicon dioxide on silicon with an oxide thickness of 90 nm or 300 nm in order to increase the contrast in visible range and to identify graphene flakes. At this point, one can locate and distinguish randomly distributed single and multilayer-graphene flakes under microscope. In this condition, thick graphene or graphite flakes appear more bluish, while few- layer and single layer-graphene will look dark and light purple respectively, as it is illustrated in figure 2.3.

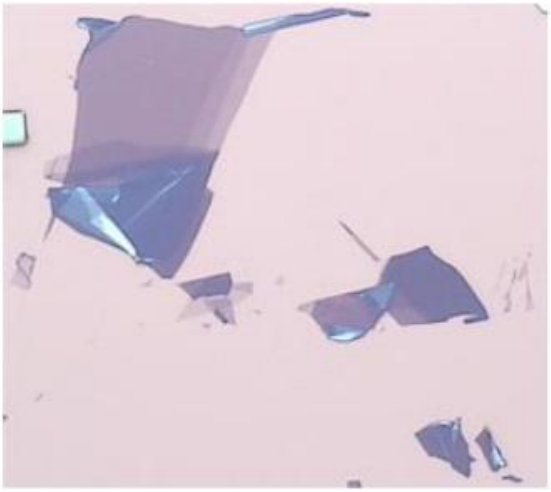


Figure 2.3: Single-layer, multi-layer, and graphite flakes on 90nm silicon dioxide on silicon substrate. Light purple shows thinner graphene.

4.2) Epitaxial Growth on Silicon Carbide Single Crystal: This approach consists of sublimation of silicon atoms from the surface layers of silicon carbide (0001) substrate at the temperature of about 1300˚C in an ultrahigh vacuum environment. Surface study shows the produced graphene layers, in this technique, are strained with limited structural coherence length, 20 nm. Although this method produces graphene in larger scale than exfoliation method does, high temperature and high cost of production are considered as serious hinder for application of this method.

4.3) Chemical Vapour Deposition: In this technique, a transition metal film such as Ni, Co, Pt, Ir or Ru is exposed to a hydrocarbon gas. Under various temperatures and pressures dependent on the substrate metal and gas type, carbon atoms dissolve into the metal surface and then force to precipitate by cooling. Several techniques have been developed to detach the produced graphene sheet from the transition metal and transfer it to an appropriate insulating substrate. CVD is a promising technique for production of large area, high quality graphene especially for flat displays and transparent electrode applications.

4.4) Self-Assembly of Soluble graphene: In this method, graphene sheets can be prepared by Two-dimensional assembly of graphene in solution phase. Deposition of graphene from the solution can be also done from reduction of graphene oxide. Although graphene obtained by this method has still relatively poor electrical quality, this technique shows the possibility of producing low cost and large-scale graphene for flexible and transparent electronics.

5. Graphene based FET fabrication

After mechanical exfoliation, i.e., the isolation of the graphene flakes it is necessary to differentiate between a single and bilayer of a stack of layers. The pioneering works which used exfoliation method to make these graphene layers, proposed the use of 300 nm of native SiO_2 on the silicon substrate so that the graphene flakes could be identified under an optical microscope by the optical contrast exhibited due to interference phenomenon. To further enhance the resolution of the flake, AFM (Atomic force microscopy) and Raman Spectroscopy is used. After characterizing and selecting suitable graphene flakes, one then proceeds to fabricate field effect transistors (FET) with graphene as conducting channel.

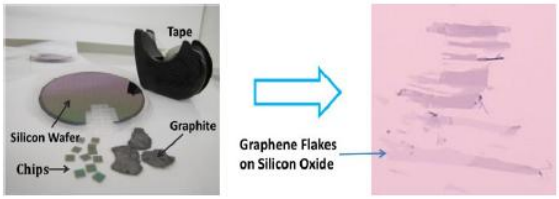


Figure 2.4: Graphene was exfoliated by adhesive tape and transferred onto the substrate (picture on the right hand side). The most transparent flakes in the picture are single layer graphene while dark purple shows thicker multilayer graphene.

5.1) Marker-assisted electron beam lithography (EBL)

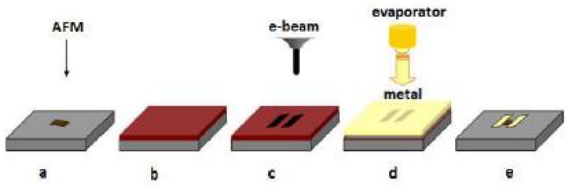


Figure 2.5: The EBL procedure represented in a schematic fashion, step-wise. (a) Characterization with AFM, (b) spincoating PMMA, (c), e-beam lithography, (d-e) evaporation and lift-off.

Electronic-beam lithography (EBL) has been the main method used for the fabrication of prototype graphene devices. This FET fabrication process usually involves a marker-based electron beam lithography technique. Its application is to prepare suitable masks on the substrate, onto which desired metal is evaporated as an electrode. In this process, electron beam sensitive resist poly-methyl methacrylate (PMMA) is spin-coated onto the substrate. PMMA is a positive resist, and when exposed to an electron beam, the polymer chains would break in the exposed areas. The regions to be exposed to the electron beam are identified by using the co-ordinates of the pre-written markers on the substrate. The marker based regions, which were hitherto identified using

optical and AFM techniques, help in the alignment between the electrode layout and the sample during the e-beam writing. These exposed regions can be preferentially dissolved in a suitable solvent like methyl iso-butyl ketone (MIBK). The sample is then put in a vacuum chamber to evaporate contact metals. One could evaporate a variety of metals, but only a select few would match the purpose of near-ohmic contacts. After the evaporation of metal contacts, the PMMA is removed in a

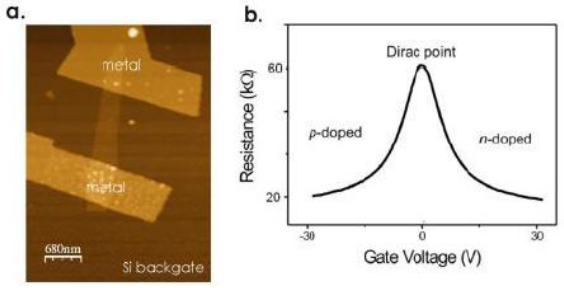


Figure 2.6: (a) AFM image of a graphene-based FET (b) The back-gate dependence plot of the FET.

solution of 1-methyl-2-pyrrolidone (550oC, 3 hours). The procedure is summarized in figure and a finished graphene-based FET can be seen in the figure. The source and drain contacts lead to larger contact pads (150 micron x 150 micron) which provide the interface to external electrical probes during electrical measurements. Since the silicon on the bottom acts as gating device, this configuration is termed as "back-gated FET". Although, EBL is the chief method still it has limitation such as scalability and being a sequential process, graphene devices like many other nano-scale devices suffer from limited industrial acceptability.

5.2) Photolithography on Graphene:

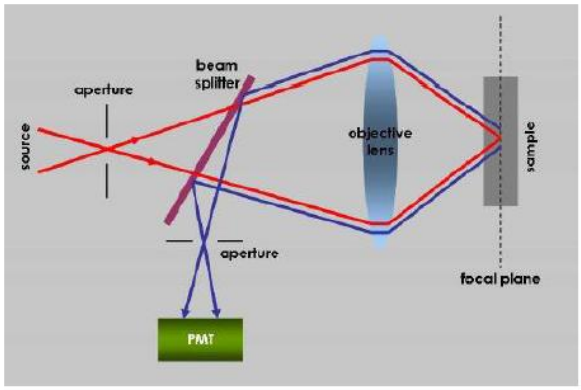


Figure 2.7: A schematic depiction of components of a Confocal Microscope.

In order to develop graphene into an application-relevant material, it is important to realize the capability of large scale production of graphene devices. Current methods described such as EBL, require the identification of graphene with the help of markers on a substrate, followed by subsequent deposition of electrodes, thereby requiring steps which involve a manual alignment procedure. The identification is performed using an optical microscope and a specified oxide thickness is necessary for obtaining the optimal contrast. Here, we demonstrate a novel strategy involving just a single process step, without the use of markers. The graphene flakes are identified and the devices are fabricated on-the-fly using a confocal laser scanning microscope. The graphene flakes were prepared by exfoliation of HOPG and then transferred onto a silicon wafer (highly p-doped) with a thermally grown 300 nm SiO_2 serving as the insulating gate dielectric. Such transfer can also be performed with sheets grown from silicon carbide, or chemically derived graphene sheets. Hence, the procedure outlined here can be adopted to all sources of graphene sheets, fabricated in any manner and on any substrate.

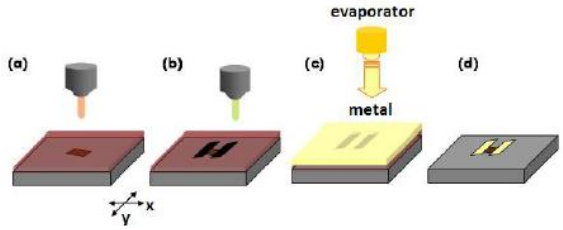


Figure 2.8: A schematic describing the steps involved in our fabrication process of a graphene-FET using photolithography.

Figure 2.8 shows a schematic describing the steps involved in our fabrication process starting from an exfoliated graphene sheet on the Si/SiO_2 substrate. The substrate is spin-coated with a photoresist (ma-P1215, micro resist technology GmbH) and baked to obtain a 1.5 mm thick film. The ma-P1215 is a G- or I-line photoresist with absorption maxima close to 436 nm or 365 nm. Illumination by UV light induces chemical changes in the resist increasing the solubility of the exposed areas, which can be preferentially stripped off by dissolution in an appropriate developer solution (ma-D331, micro resist GmbH). A subsequent metal evaporation step and a lift-off procedure finalize the device fabrication providing metal regions only in the exposed areas. Usually, a mask is used to specify the layout of the electrodes. Although ma-P1215 is designed for UV exposure, we have observed that the coated resist still possesses a sizeable molar absorption coefficient up to visible wavelengths of around 580 nm. Chemical modifications can still be induced by irradiating with low energy laser sources. We exploit this property to devise a fabrication protocol, wherein the exposure is performed at a wavelength of 476 nm (write laser) instead of UV light. On the other hand, at a wavelength of 633 nm (imaging laser), the sample can be imaged without chemically modifying the photoresist. Thus obtained confocal images enable identifying the flakes as depicted in Figure 2.8b.

After the flake is identified, the write laser is utilized to perform the exposure. The desired layout is obtained by scanning the piezo stage using a computer controlled interface, avoiding the need for a separate mask. After a

development step the desired metal is evaporated onto the sample (Figure 2.8c). The procedure is completed (Figure 2.8d) by removing the residual photoresist by lift-off in 1-methyl-2-pyrrolidone (55oC for 3 hours), thus yielding a graphene-based transistor.

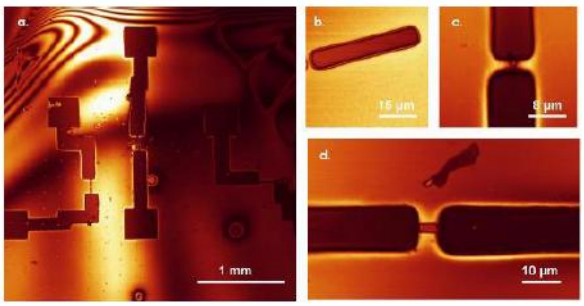


Figure 2.9: Confocal reflection images showing different sizes of exposure.

III. SILICON FETS VIS-À-VIS GRAPHENE BASED FET

Any transistor based on an alternative material (other than silicon) must compete with a 50-odd year history of MOSFETs. The FETs usually rely on a heavily doped silicon wafer that is used as back-gate electrode and as the substrate. The substrate is coated with an insulating layer called gate dielectric. In contrast, the graphene FETs that are being addressed in this thesis are not deliberately doped, and the channel is formed by the accumulation of holes or electrons, with the underlying Si/SiO_2 substrate acting as the back-gate.

For high-speed applications, FETs should respond quickly to variations in gate voltage, which requires short gates and highly mobile carriers in the channel. Unfortunately, FETs with short gates suffer from degraded electrostatics and other problems (collectively known as short-channel effects), such as threshold-voltage roll-off, drain-induced barrier lowering, and impaired drain-current saturation. Scaling theory predicts that a FET with a thin barrier and a thin gate-controlled region will be robust against short-channel effects down to very short gate lengths. The possibility of having channels that are just one atomic layer thick is perhaps the most attractive feature of graphene for use in transistors.

The channels in III-V group High Electron Mobility Transistors (HEMTs) are typically 10 to 15 nm thick, and although silicon-on-insulator MOSFETs with channel (that is, silicon body) thicknesses of less than 2 nm have been reported, rough interfaces caused their mobility to deteriorate. More importantly, the body of these MOSFETs showed thickness fluctuations that lead to unacceptably large threshold-voltage variations (and similar problems are expected to occur when the thickness of the channel in a III- V HEMT is reduced to only a few nanometers). These problems occur at thicknesses that are many times greater than the thickness of graphene. The series resistances between the channel and the source and drain terminals are also important, and their adverse impact on the FET becomes more pronounced as the gate length decreases. As a result, device engineers devote considerable effort to developing transistor designs in which short-channel effects are suppressed and series resistances are minimized.

Current digital logic is based on silicon complementary metal oxide semiconductor (CMOS) technology, which includes gates consisting of both n- and p-channel MOSFETs that can be switched between the on-state (i.e. with a large on-current, Ion, and Vgs =+-Vdd, where Vdd is the maximum voltage supplied to the device) and the off-state (with a small off-current, Ioff, and Vg = 0). In other words, the gate terminal is involved in the logical operation.

Power dissipation is another key issue in CMOS technology. The ability to switch off silicon MOSFETs enables extremely low static power dissipation. In the steady state, a certain number of the MOSFETs in a CMOS logic gate are always switched off so that no current, except the small Ioff flows through the gate. Thus, according to ITRS, any successor to the silicon MOSFET that is to be used in CMOS-like logic must have excellent switching capabilities, as well as an on/off ratio, Ion/Ioff , of between 104 and 107. In a conventional FET, this would require semiconducting channels with a sizeable band gap, preferably 0.4 eV or more. Moreover, n- and p-channel FETs with symmetrical threshold voltages, that is, with VThn = -VThp, are needed for proper CMOS operation. Thus, in this scenario graphene receives a blow, due to its semi metal characteristic and though now, things are getting resolved by using methods to induce a band gap by the methods such as substrate induction.

In radiofrequency (RF) applications, however, such a switch-off is not required. In small-signal amplifiers, for example, the transistor is operated in the on-state and small radiofrequency signals that are to be amplified are superimposed onto the D.C. gate/source voltage. The cut-off frequency (fT) is the frequency at which the magnitude of the small signal current gain rolls off to unity. The cut-off frequency is the most widely used figure of merit for radiofrequency devices and is, in effect, the highest frequency at which a FET is useful in radiofrequency applications .For GaAs HEMTs, Vds, has a pronounced effect on the FET performance. Typically in such transistors, fT peaks around Vds = 1 V, that is, deep in the region of drain-current saturation, where gm is near its peak and gds has decreased sufficiently. For lower values of Vds, the device operates in the linear regime and the cut-off frequency is low because gm is small and gds is large. The critical issue for radiofrequency performance is that although shorter gates, faster carriers and lower series resistances all lead to higher cut-off frequencies, saturation of the drain current is essential to reach the maximum possible operating speeds. Transistors made from graphene also have a very high cut-off frequency above 100GHz and show low levels of noise. The fastest graphene transistor

reported so far is a MOSFET with a 240 nm gate that has a cut-off frequency of fT = 100 GHz, which is higher than those of the best silicon MOSFETs with similar gate

lengths (so is the cut-off frequency of 53 GHz reported for a device with a 550 nm gate). A weak point of all radiofrequency graphene MOSFETs reported so far is their unsatisfying saturation behaviour (only weak saturation or the second linear regime), which has an adverse impact on the cut-off frequency, the intrinsic gain and other figures of merit for radiofrequency devices. Nevertheless, outperforming silicon MOSFETs while operating with only weak current saturation is certainly impressive.

IV. GRAPHENE FET PHYSICS

1. Evolution of Graphene FET

A graphene MOS device was among the breakthrough results reported by the Manchester group in 2004. A 300-nm SiO2 layer underneath the graphene served as a back-gate dielectric and a doped silicon substrate acted as the back-gate (Figure 4.a). Such back-gate devices have been very useful for proof-of-concept purposes, but they suffer from unacceptably large parasitic capacitances and cannot be integrated with other components. Therefore, practical graphene transistors need a top-gate. The first graphene MOSFET with a top-gate was reported in 2007, representing an important milestone, and progress has been very rapid since then (Figure 4.b).

2. Current-Voltage Characterics of GFETs

Due to the gapless property of graphene, typical GFETs exhibit ambipolar behaviour in which charge carriers change from electrons to holes and vice versa at a minimum conductivity point called Dirac neutrality point. In an ideal case, the transfer characteristic of GFET should be quasi ballistic. However, device fabrication and structure introduce limitations that make us to use drift-diffusion model to describe drain current. Also, some of these limitations such as source and drain contacts can be the origin of asymmetric transfer characteristics in some cases.

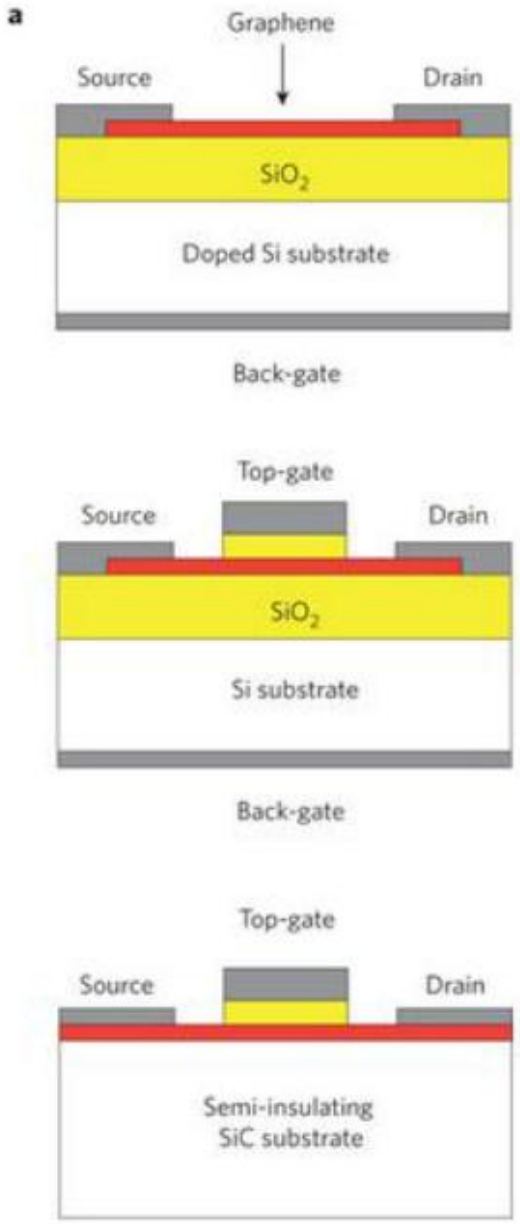


Fig. 4.a. Schematics of different graphene MOSFET types: back-gated MOSFET (left); top-gated MOSFET with a channel of exfoliated graphene or of graphene grown on metal and transferred to a SiO2-covered Si wafer (middle); top-gated MOSFET with an epitaxial-graphene channel (right). The channel shown in red can consist of either large-area graphene or graphene nanoribbons.

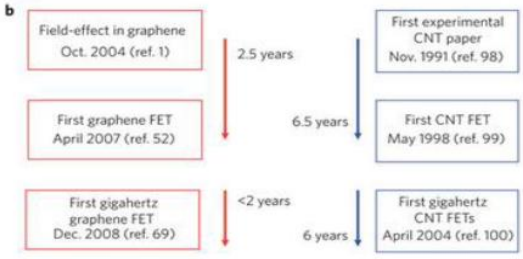


Fig. 4.b. Progress in graphene MOSFET development compared with the evolution of nanotube FETs.

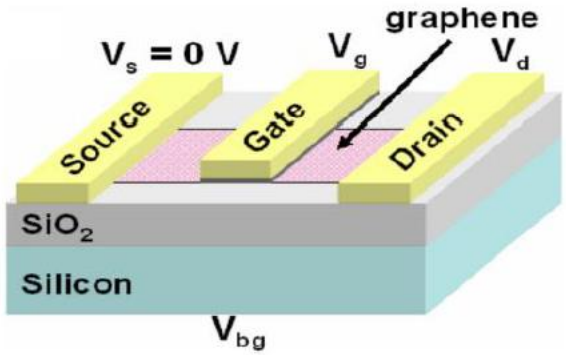


Fig. 4.2: Schematic of dual gate graphene field effect transistor.

In recent years, several models for current-voltage characteristics of GFETs have been proposed. For instance, a model tries to fit current voltage characteristics of GFET to that of conventional MOSFET. In this model, at low drain voltages (Vds<Vgs-V0), drain current can be described by equation in which a constant charge carrier mobility is assumed.

$$I_d = \frac{W}{L}\mu C_{ox}\left[(V_{gs} - V_0)V_{ds} - \frac{V_{ds}^2}{2}\right]$$

This equation is the same as MOSFET drain equation except for V0 which is the Dirac neutrality point in GFETs. In addition, there is always a minimum conductivity point much larger than the universal minimum conductivity ($4e^2/h$) due to inhomogeneity and thermal excitations. Thus, the minimum conductivity should be considered in the transport model.

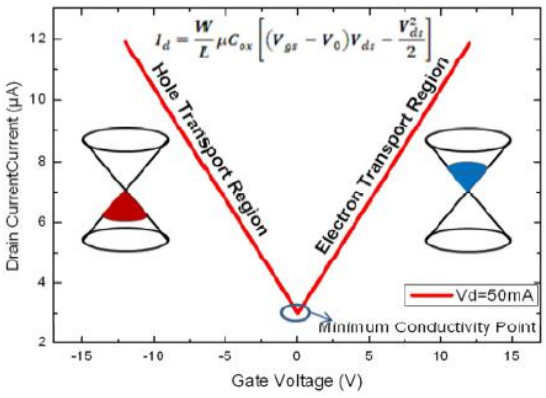
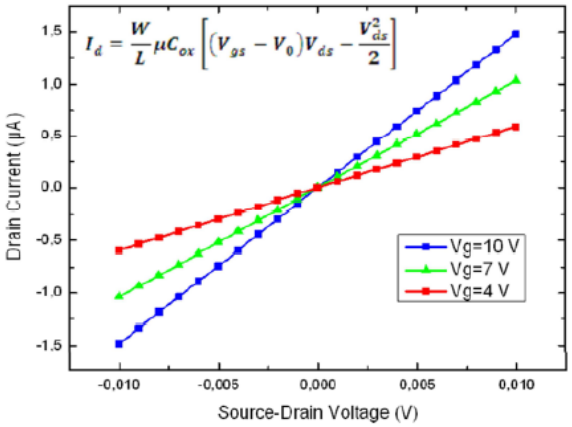


Fig. 4.3: Simulated ideal drain current versus gate voltage.

Figure 4.3 shows the simulated transfer characteristic of graphene field effect transistor using equation 2-1, and a minimum conductivity. The V-shape of transfer characteristics reflects the ambipolar transport behaviour of GFETs. The ideal output characteristics of GFETs at low field ($V_{ds}<V_{gs}-V_0$) exhibits linear behaviour as shown in figure 4.4.



4.4: Simulated ideal drain current against source-drain voltage for different gate biases.

V. OUTLOOK TOWARDS APPLICATIONS

In spite of some fundamental shortcomings, graphene FETs still have progressed very briskly towards probable applications. In May 2009, teams from Stanford University,

University of Florida and Lawrence Livermore National Laboratory announced that they have created an n-type transistor, which means that both n- and p-type transistors have now been realized in graphene. A month later, researchers at the Politecnico di Milano demonstrated the first graphene integrated circuit, a complementary inverter consisting of one p- and one n-type graphene transistor. Late in 2010 the first graphene based triple-mode single-transistor was fabricated. The fore mentioned are considered to be important steps into building very basic circuits using graphene. The latter two especially have been cited as the primary steps towards building a functional circuit using graphene unfortunately while inverters and amplifiers are essential components in building a circuit, their respective 'gain' must be greater than unity to be useful , the graphene inverters reported to date suffer from a very low voltage gain.

VI. FINAL REMARKS

Graphene-based nano electronics is still in its infancy to make any valid conclusions as there is very long way to go before it can challenge the 50-odd year old CMOS technology. The concepts that have been investigated for many years now, like spin transistors or molecular devices, seem to be farther from real application when you compare them to advancements in graphene, and it is not clear if they will ever reach the production stage. It has become clear that graphene devices based on the conventional MOSFET principle suffer from some fundamental problems and still certain principle questions like on/off ratios and mass-scale production need to be tackled. However, it is worth remembering that the research on graphene is addressed as a replacement technology. This or even the more novel and alternate FET designs like tunnel FETs and bilayer

pseudo spin FETs would have to outperform CMOS technology by many orders to replace an existent technology, which has a whole industry invested in it. At the moment though, it would not be possible to say which (if any) of the alternative concepts being considered will replace conventional transistors. Nonetheless, the latest ITRS roadmap strongly recommends intensified research into graphene, and even envisions a research and development schedule for carbon-based nano electronics. The work in this field is only beginning. And the expectations are high.

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