Abstract: Spurious Power Suppression Technique (SPST) is a technique used for reducing the power in VLSI circuits by neglecting the unwanted or spurious signals present at the input. The proposed SPST separates the target design into two parts, i.e., the most significant part and least significant part (MSP and LSP) and turns off the MSP when it does not affect the computational result to save power. This technique dramatically reduces the power dissipation in multimedia/DSP application design examples, i.e., versatile multimedia functional unit (VMFU) and FIR Filters. In this project we specifically reduce the power consumed by the multipliers present in FIR Filters using Modified Booth Encoding Algorithm combined with SPST. It also adopts the optimization of number of cells present in the design. The proposed design of SPST in FIR Filter will be designed using Verilog HDL and synthesized, implemented using Cadence ASIC Tools.

Keywords: FIR, Booth Algorithm, Low Power Design

I. INTRODUCTION

One of the accompanying challenges in designing ICs for portable electrical devices is lowering down the power consumption to prolong the operating time on the basis of given limited energy supply from batteries[7]. Owing to the vigorous development of the wireless infrastructure and the personal electronic devices like video mobile phones, mobile TV sets, PDAs, etc., multimedia and DSP applications have been adopted.

Various techniques have been developed for reducing the power consumption of VLSI designs, including voltage scaling, switched-capacitance reduction, clock gating, power down techniques, threshold voltage controlling and dynamic voltage frequency scaling. These low-power techniques have been proven to be efficient at certain expense and are applicable to multimedia/DSP designs. Among these low power techniques, a promising direction for significantly reducing power consumption is reducing the dynamic power which dominates total power dissipation. The proposed low-power technique can be used with some of the aforementioned techniques without conflicts to further reduce the power consumption of the multimedia/DSP designs.

Consequently, a new low power technique which can reduce dynamic power consumption includes a concept called partially guarded computation which divides the arithmetic units into two parts and turns off the unused part to minimize the power consumption called as the spurious power suppression technique (SPST). This technique is implemented in the multipliers of digital FIR filters.

II. PROPOSED SPST

Spurious Power Suppression Technique is technique used for reducing the power in VLSI circuits by neglecting the unwanted or spurious signals present at the input. The spurious power suppression technique separates the target design into two parts i.e., the MSP and LSP and turns off the MSP when it does not affect the computational results to save the power. The SPST can dramatically reduce the power dissipations of combinational VLSI circuits such as the multimedia/DSP processors. The data of the multimedia/DSP computations tend to fluctuate within a small range of bit width due to spatial redundancies. When the SPST is applied on combinational circuitries, we should first determine the longest transitions of the interested cross sections of each combinational circuitry, which is timing characteristic.

The proposed SPST [5] can decrease the switching power dissipation comprising of a significant portion of the complete power dissipation in integrated circuits. Furthermore, the proposed SPST is a fully static circuit technique which does not aggravate the problems of leakage power, signal racing and voltage dropping.

III. SPST DESIGN FOR FIR FILTERS

Finite impulse response (FIR) filters are widely used in various DSP applications [4]. As the name implies, an FIR filter consists of a finite number of sample values. An FIR filter with constant coefficients is an LTI digital filter. The output $y[n]$ of an FIR filter of length $N$ is given by:

$$y[n] = \sum_{k=0}^{N-1} h[k] x[n-k]$$

where $x[n]$ are the input samples, $h[k]$ are the filter coefficient samples.
Thus the FIR Filter implemented is as shown in the figure below:

As shown in the fig 1 above the FIR Filter consists of mainly three components as mentioned below:

- Multipliers
- Adders
- Delay Unit

The above given example is implemented using the SPST technique[5]. In this example the MSP of the multiplier is a zero signal or unwanted and hence while recoding the multiplier the MSP is neglected by not multiplying it with the multiplicand and just directly passing the previous output as the partial products are added simultaneously when it is generated. So this technique of ignoring the spurious signal is called SPST in multiplier of Radix4 Booth algorithm. Thus the power is reduced along with thereduction in number of partial products when compared to other multipliers.

IV. IMPLEMENTATION DETAILS

The tool used for implementing this technique is Cadence ASIC tools.

The three main steps involved in ASIC design flow is:

- Functional Simulation
  - The tool used is Incisive Enterprise Simulator (IES).
- Synthesis
  - The tool used is RTL compiler (RC).
- Physical Design
  - The tool used is Encounter Digital Implementation (EDI).
V. RESULTS

In order to verify experimentally the proposed scheme the desired system is implemented in Cadence ASIC tools.

Our results are classified into the following categories:

A) SIMULATION WAVEFORM

Fig 5: Simulation result of 4-tap FIR filter using booth multiplier

Fig 6: Simulation result of 8-tap FIR filter using booth multiplier

B) SYNTHESIS OUTPUT

Fig 7: Synthesis result of FIR filter using booth multiplier

Fig 8: Power consumption of 4-tap FIR Filter using Booth Multiplier

Fig 9: Power consumption of 8-tap FIR Filter using Booth Multiplier
Fig 10: Report timing of 4-tap FIR Filter using Booth Multiplier

Fig 11: Report timing of 8-tap FIR filter using Booth multiplier

C) PHYSICAL DESIGN

Fig 12: Physical Design of FIR filter using booth multiplier

D) RESULT ANALYSIS

The following table shows comparison of power consumption and number of cells used between basic FIR filter and FIR filter using Modified Booth.

<table>
<thead>
<tr>
<th>Instance</th>
<th>Cells</th>
<th>Leakage Power (mW)</th>
<th>Dynamic Power (mW)</th>
<th>Total Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic FIR Filter-4 tap</td>
<td>1101</td>
<td>1067.708</td>
<td>5332882.122</td>
<td>5333944.900</td>
</tr>
<tr>
<td>FIR Filter using SPST-4 tap</td>
<td>853</td>
<td>1678.499</td>
<td>465609.192</td>
<td>466065.390</td>
</tr>
<tr>
<td>Basic FIR Filter-8 tap</td>
<td>2455</td>
<td>4036.696</td>
<td>1597779.712</td>
<td>1601956.930</td>
</tr>
<tr>
<td>FIR Filter using SPST-8 tap</td>
<td>39309</td>
<td>3847.302</td>
<td>1196586.373</td>
<td>1199433.706</td>
</tr>
</tbody>
</table>

Fig 14: Comparison of power consumption between basic fir filter and fir filter using Booth

From the comparison it is seen that the FIR filter using the SPST saves around 12% power in case of a 4tap filter and around 23% power in case of 8tap filter.

VI. CONCLUSION

This project proposes a low power technique called SPST and explores its applications in multimedia/DSP computations [4] where the theoretical analysis and the realization issues of the SPST are fully discussed. The proposed SPST can obviously decrease the switching (or dynamic) power dissipation, which comprises a significant portion of the whole power dissipation in integrated circuits. To reduce power consumption and the number of cells we use the Modified Booth Encoding Algorithm combined with Spurious Power Suppression Technique (SPST) [5]. The proposed FIR filters have been designed using Verilog HDL, synthesized and implemented using CADENCE ASIC TOOLS.

The different application that uses this technique is multimedia and DSP designs which are MP3 players, iPod players, iPad, Kindle, video processing(video players, video streamers), video mobile phones, mobile TV sets, PDAs, H.264 CODECs, audio Compression, speechprocessing(microphones, voice recorders) and image processing.

The advantages of this technique is that it reduces power consumption, sustains the operating time, lower expense in manufacturing the device, highly reliable.

VII. ACKNOWLEDGEMENT

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