10 Bit 500 MHz Current Steering DAC

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Abstract—A 10 bit, 500MHz segmented current steering Digital to Analog converter is designed. The DAC is implemented using 90nm technology with a supply voltage of 1.2 V. The design is implemented with the matching network, required for the current sources. Segmented architecture of the DAC is used in order to decrease the glitch and to improve the monotonicity, even though that increases the cost. The spurious free dynamic range (SFDR) and signal to noise and distortion ratio (SNDR) performances of the segmented DAC architecture is also analyzed in this paper.

I. INTRODUCTION

In application like wireless communication, digital video and audio requires effective data converters that can achieve higher speed or conversion rate and resolution. Thus a wide range of digital to analog converter(DAC) exists, each have its own advantage. The current-steering DACs can achieve high conversion rate and thus are used in high frequency signals.

This type is called current-steering DAC since it uses current throughout the conversion as compared to other DACs where a voltage is converted into current which is then used to generate voltage at the output. Current-steering type of DACs requires precision current sources that are summed in various fashions. Current-steering DACs have one advantage of high current drive inherent in the system and, since output buffers are not required to drive resistive load this DACs are used in high speed applications. To achieve good linearity and less glitch energy, segmented architecture of the DAC is implemented here.

II. DAC ARCHITECTURE

We can use different type of architectures fir DAC such as voltage dividers , segmented DAC, R -2R ladder DACs and Delta sigma architecture. Fig.1 shows the block diagram of a conventional 10 bit current steering DAC. To achieve good linearity and less glitch energy, segmented architecture of the DAC is implemented here. In the thermometer-code implementation, each unit current source is connected to a switch controlled by the signal coming from the binary to thermometer decoder. When the digital input is increases from 1 LSB, one more current source is switched from the negative to the positive side. Thus the monotonicity is guaranteed by using this architecture . At the mid-code a 1 LSB transition causes only one current sources to the switch as the digital input only increases by one. This will reduces the glitch problem. Glitches hardly contribute to the non-linearity in the thermometer coded DAC. [1] One major drawback of the thermometer coded DAC is the area and power consumption. To

Fig. 1. Basic block diagram of DAC
a DFF. In the first step of decoding, the binary code is decoded into a row and column decoder. The selection of the current cell is correspond to the input value of the row and column decoder. The output of the switching logic is given to the DFF and this will go as an input to the current cell.

Fig. 2. Circuit diagram of unit current cell

Fig. 3. Biasing circuit

III. CURRENT CELL AND SWITCHING LOGIC

When a MOS transistor is used as switch in a conventional current cell, the signal on the gate can couple to the output through the gate to drain capacitance. In the current cell two cascaded current sources are applied to increase the output impedance and the input signal to the switching transistors D and DB are opposite in logic. The low to high transition to one the transistor bring in to the linear region and the other will in the off mode. The problem of output voltage variation of the current source can be decreased by placing a cascade transistor on the top of the switch [2]. For a low to high transition of the control signal, while the switching transistor is forming a channel, the cascade transistor are off and the signal path from the drain of the switching to the output node is open. The cascade current source also improve the input resistance of the current source, so the output voltage variation can be suppressed. The switching logic for successive selection of the current cell is modeled using the OR gate and NAND gate. The input to the selection logic will be the thermometer code that will corresponds to number of current cells.

Fig. 4. Decoding logic for each current cell

IV. BINARY TO THERMOMETER DECODER

The binary code is decoded into a row and column decoder. Each this row decoder and column decoder will have 32 output lines each with a 5 bit input. By the combination of the row decoder and column decoder the turn on of the 1024 current cell made possible [3]. The thermometer code T0 to T31 is implemented using AND and OR gates.

\[
\begin{align*}
T32 &= a \cdot b \cdot c \cdot d \cdot e \\
T31 &= a \cdot b \cdot c \\
T29 &= a \cdot b \cdot c \cdot (d + e) \\
\vdots \\
T1 &= a + b + c + d + e
\end{align*}
\]

Fig. 5. Decoding logic with an example

V. COMPLETE CURRENT BLOCK IN THE THERMOMETER CODED DAC

The complete current block used in the thermometer coded DAC is shown in the figure it will have a

Fig. 6. Simple resistive load at the output
switching logic and the output of that will go to the DFF so that it will shift the crossing of the switching transistor only at the clock edge. The output of the DFF will go to the switches. A single

Fig. 7. Transimpedance logic at the output
resistor at the output converts current into voltage. Here we are using 50 ohm resistor. In this case, the fullscale output current is enough to produce responsible voltage swing across resistor. Due to parasitic capacitance, the node will experience the entire output voltage swing. We can replace resistor with a transimpedance amplifier so that voltage variation at the node will be less. Output settling will be determined by the op amps speed (ideal opamp have high impedance at the node connected to current steering DAC) [4]. Because of this reason non-linearity will be less and this system will provide better SFDR.

VI. SIMULATION RESULTS

![Fig. 8. Differential output with flip-flop](image)

VII. CONCLUSION

The Current Steering DAC using Segmented Architecture is designed in 90 nm technology. It has been observed that SFDR and SNDR is more when we replace the resistor at the output by transimpedance amplifier. When we increase the gain of transimpedance amplifier, due to virtual ground property of opamp SFDR is increasing. The area and power consumption of current steering DAC is more.

![Fig. 9. Transimpedance logic at the output](image)

![Fig. 10. FFT of current steering DAC with simple load resistor](image)

![Fig. 11. FFT of differential output using transimpedance amplifier with gain of 40 dB](image)

Table 1: Comparison of SFDR for Different DAC Architectures

<table>
<thead>
<tr>
<th>Type of architecture</th>
<th>SNDR (dB)</th>
<th>SFDR (dB)</th>
<th>ENOB (bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Segmented DAC with 50 Ω resistor</td>
<td>40.71dB</td>
<td>40.785dB</td>
<td>6.48</td>
</tr>
<tr>
<td>DAC with TIA of 40dB gain</td>
<td>60.093dB</td>
<td>72.78dB</td>
<td>9.76</td>
</tr>
<tr>
<td>DAC with TIA of 60dB gain</td>
<td>61.44dB</td>
<td>75.73dB</td>
<td>9.91</td>
</tr>
</tbody>
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REFERENCES

