



LOW POWER ANALOG TO DIGITAL CONVERTOR FOR COMPUTATION TECHNIQUES

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Abstract - Reducing power dissipation is very important for portable battery powered devices such as digital cameras, cell phones, laptop PCs, etc. The analog to digital data converter is one of the most commonly used building blocks of analog and mixed signal circuits used in such devices. The major reason for using a power scalable architecture is to consume as less power as possible. An architecture can work optimally only for a range of bandwidths for some specific clock frequency. For making them work at different speeds, a method is needed to change their bandwidth in an efficient way. There are two strategies for creating such a wide operating range digitization system: One option is to employ a single very high performance ADC that can work at the highest common denominator of resolution and sampling rate. This would be either infeasible or extremely power inefficient. The second strategy is to employ multiple A/D converter architectures each specified to cover a small sector in the entire two dimensional resolutions and sampling rate space. The main objective of the project is a novel Analog-to-Digital architecture for high speed applications that is compatible with digital CMOS and surpasses the issues with traditional voltage conversion techniques. A delay line based ADC with 7mW power consumption is designed in 250nm CMOS based on the proposed architecture using T-Spice.

Keywords – VLSI, MOSFET circuits, MOS logic circuits, MOS integrated circuits

I. INTRODUCTION

The emergence of high speed wire line and wireless protocols combined with the increase in low cost CMOS technology which is widely in favor of digital processing has put a high desire toward more digitally-assisted high speed applications. These applications vary from UWB standards and RF signal sensing in wireless transceivers to wire line signal conditioning and data acquisition [1]. Analog-to-digital converters are the major challenge for these digitally-assisted applications. Because of the nature of these applications an ultra high speed ADC with a relatively low number of bits is

required. Even though the accuracy is low but because of the high speed required for processing the analog signal, the power consumption of these blocks become extremely important. The conventional architectures for this range of ADCs are mostly high speed flash [1], folding flash [6], Successive Approximation (SAR) Converters and Pipeline structures[3]. The flash topology, along with its interpolating and folding variants, has been the conventional choice for high-speed, low resolution ADCs. While flash can maintain the highest throughput, it requires an exponential growth in the number of comparisons with the resolution. Pipelined ADCs are used for high-speed, medium-resolution applications. They can provide one conversion per clock period throughput and only a linear scaling in complexity with resolution; however, they rely on operational amplifiers at the heart of the multiplying digital-to-analog converter (MDAC) in each pipelined stage. Because it must be closed loop stable, this amplifier typically uses one or two high gain stages. Unfortunately, in deep-submicron CMOS, the achievable gain per stage is limited because short-channel effects lower for a single transistor, and reduced voltage supplies restrict circuit techniques such as cascading. Thus, there are significant challenges for continued scaling of pipelined ADCs. Very recently, for the high-speed, low resolution converters necessary for UWB, the time-interleaved successive approximation register (SAR) architecture has re-emerged as a low-power alternative to flash and pipelined ADCs. At the required speeds, their major limitation is digital power; a SAR converter includes digital feedback in the critical path. A full custom logic controller with dynamic registers can reduce digital power significantly, but it still remains a dominant source of power consumption in a 0.18-um CMOS implementation [4].

Analog-to-Digital conversion is performed in three steps: signal difference amplification, a zero crossing

detector and a succeeding logic encoder. The analog signal difference amplification in all mentioned architectures are performed by amplifying the analog voltage (current) level by a voltage (current) amplifier. Due to the voltage and device scaling in the mainstream CMOS technology, both amplification and comparison are becoming more and more challenging mainly because the devices should be large and power hungry for large gain and low offset. We use delay amplification as a different solution for signal difference amplification that shows significantly better performance for the high speed low resolution end of the ADC application spectrum.

Literature Survey

A direct-conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, capable of gigahertz sampling rates, but usually has only 8 bits of resolution or fewer, since the number of comparators needed, $2^N - 1$, doubles with each additional bit, requiring a large, expensive circuit. A Pipeline ADC uses two or more steps of sub ranging. First, a coarse conversion is done. In a second step, the difference to the input signal is determined with a digital to analog converter (DAC). This difference is then converted finer, and the results are combined in a last step. This can be considered a refinement of the successive-approximation ADC wherein the feedback reference signal consists of the interim conversion of a whole range of bits rather than just the next-most-significant bit. By combining the merits of the successive approximation and flash ADCs this type is fast, has a high resolution, and only requires a small die size.

The successive approximation Analog to digital converter circuit typically consists of four chief sub circuits: A sample and hold circuit to acquire the input voltage (V_{in}). An analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR). A successive approximation register sub circuit designed to supply an approximate digital code of V_{in} to the internal DAC. An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with V_{in} .

An integrating ADC applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period. The run-down time measurement is usually made in units of the converter's

clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution. Converters of this type are used in most digital voltmeters for their linearity and flexibility.

A sigma-delta ADC oversamples the desired signal by a large factor and filters the desired signal band. Generally, a smaller number of bits than required are using a Flash ADC after the filter. The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies. A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output (sigma-delta modulation, also called delta-sigma modulation).

A Time-interleaved ADC uses M parallel ADCs where each ADC sample data every Mth cycle of the effective sample clock. The result is that the sample rate is increased M times compared to what each individual ADC can manage. In practice, the individual differences between the M ADCs degrade the overall performance reducing the SFDR. However, technologies exist to correct for these time-interleaving mismatch errors.

All the above mentioned ADCs which work on voltage comparison are having either high accuracy or high speed. None of the ADCs are having both the parameters high. The proposed delay line ADC has high speed and accuracy. The comparison table of different types of ADC based on its speed and accuracy is shown below.

Low-To-Medium speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low-To-Medium Accuracy
Integrating	Successive Approximation	Flash
Oversampling	Algorithmic	Pipeline

Table 1: Comparisons of ADCs

II. SUCCESSIVE APPROXIMATION REGISTER (EXISTING ADC)

The successive approximation Analog to digital erter circuit typically consists of four chief sub circuits: A sample and hold circuit to acquire the input voltage (V_{in}). An analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR). A successive approximation register sub circuit designed to supply an approximate digital code of V_{in} to the internal DAC. An internal reference DAC that supplies the comparator with an analog voltage

equivalent of the digital code output of the SAR for comparison with V_{IN} .

The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{IN} the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion (EOC).

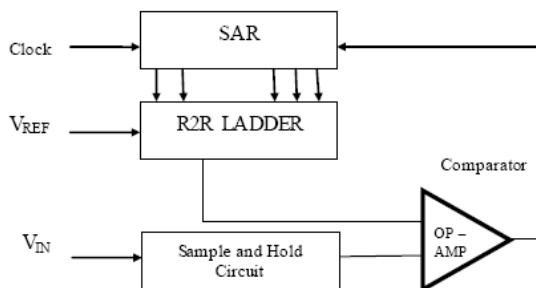


Fig 1: Successive Approximation Register ADC

Although there are many variations for implementing a SAR ADC, the basic architecture is quite simple. The analog input voltage (V_{IN}) is held on a track/hold. To implement the binary search algorithm, the N-bit register is first set to midscale (where the MSB is set to 1). This forces the DAC output (V_{DAC}) to be $V_{REF}/2$, where V_{REF} is the reference voltage provided to the ADC. A comparison is then performed to determine if V_{IN} is less than, or greater than, V_{DAC} . If V_{IN} is greater than V_{DAC} , the comparator output is logic high, or 1, and the MSB of the N-bit register remains at 1. Conversely, if V_{IN} is less than V_{DAC} , the comparator output is logic low and the MSB of the register is cleared to logic 0. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is complete and the N-bit digital word is available in the register. A SAR ADC is slower than a Flash ADC because the output bits are generated over multiple clock cycles but it uses fewer components because only a single comparator is necessary and there is no need for an encoder to translate the thermometer codes into binary. The successive approximation ADC is designed in 250nm technology using T-Spice tool.

a) Comparator

A comparator is a device that compares two voltages or currents and switches its output to indicate which is larger. They are commonly used in devices such as Analog-to-digital converters (ADCs). An operational

amplifier has a well balanced difference input and a very high gain. This parallels the characteristics of comparators and can be substituted in applications with low-performance requirements. In theory, a standard op-amp operating in open-loop configuration (without negative feedback) may be used as a low-performance comparator. When the non-inverting input (V_+) is at a higher voltage than the inverting input (V_-), the high gain of the op-amp causes the output to saturate at the highest positive voltage it can output. When the non-inverting input (V_+) drops below the inverting input (V_-), the output saturates at the most negative voltage it can output. The op-amp's output voltage is limited by the supply voltage. An op-amp operating in a linear mode with negative feedback, using a balanced, split-voltage power supply, (powered by $\pm V_S$) its transfer function is typically written as: $V_{out} = A_o(V_1 - V_2)$. However, this equation may not be applicable to a comparator circuit which is non-linear and operates open-loop (no negative feedback). In practice, using an operational amplifier as a comparator presents several disadvantages as compared to using a dedicated comparator.

b) R2R Ladder

A resistor ladder is an electrical circuit made of repeating units of resistors. An R-2R Ladder is a simple and inexpensive way to perform digital-to-analog conversion, using repetitive arrangements of precision resistor networks in a ladder-like configuration. Bit a_{n-1} MSB (most significant bit) to Bit a_0 LSB (least significant bit) are driven from 0 volts (logic 0) and V_{ref} (logic 1). The R-2R network causes the digital bits to be weighted in their contribution to the output voltage V_{out} . For example, let us consider 5 bits (bits 4-0), giving (2^5) or 32 possible analog voltage levels at the output. Depending on which bits are set to 1 and which to 0, the output voltage (out) will be a corresponding stepped value between 0 volts and (V_{ref} minus the value of the minimum step, Bit0). The actual value of V_{ref} (and 0 volts) will depend on the type of technology used to generate the digital signals.

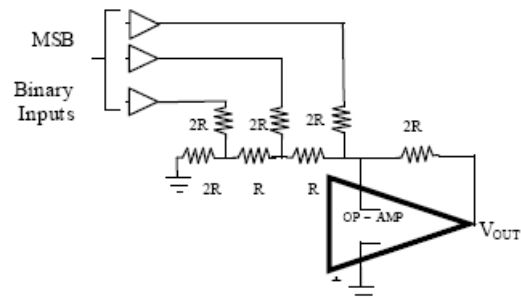


Fig 2 : R2R Ladder

The R-2R ladder is inexpensive and relatively easy to manufacture since only two resistor values are required. It is fast and has fixed output impedance R . The R-2R

ladder operates as a string of current dividers whose output accuracy is solely dependent on how well each resistor is matched to the others. Small inaccuracies in the higher significant bit resistors can entirely overwhelm the contribution of the less significant bits. This may result in non-monotonic behavior at major crossings, such as from 01111 to 10000. Depending on the type of logic gates used and design of the logic circuits, there may be transitional voltage spikes at such major crossings even with perfect resistor values. Finally, the $2R$ resistance is in series with the digital output impedance. High output impedance gates (e.g., LVDS) may be unsuitable in some cases. For all of the above reasons, this type of DAC tends to be restricted to a relatively small number of bits, although integrated circuits may push the number of bits to 14 or even more, 8 bits or fewer is more typical.

III. DELAY LINE BASED ADC (PROPOSED)

In most analog-to-digital converters (ADCs), the input analog voltage is converted into a digital code by an explicit voltage comparison. However, when integrated circuit fabrication technologies (e.g. CMOS) reach the deep sub micrometer regime, circuits that process analog voltage signals encounter scaling impediments. In particular, due to supply voltage reduction, the voltage domain is becoming noisier. In addition, the relatively high threshold voltage makes the available headroom very small for any sophisticated analog architectures. On the positive side of scaling, with rising and falling times on the order of 10 ps, the switching characteristics of MOS transistors offer excellent timing accuracy at high frequencies.

A new design paradigm with deep sub micrometer CMOS technologies is possible, in which the time-domain resolution of a digital signal edge transition is superior to the voltage resolution of an analog signal. This, along with considerations of chip area and power dissipation, gives rise to an upcoming trend to digitize part of or even the whole mixed-signal blocks. These encourage us to study ADC structures based on digital blocks and compatible with scaling. Functionally, ADCs are quite similar to time-to-digital converters (TDCs), which are used to quantize time intervals in applications such as phase-locked loops. A digital delay line-based TDC approach has recently become attractive, particularly for deep-sub micrometer technologies.

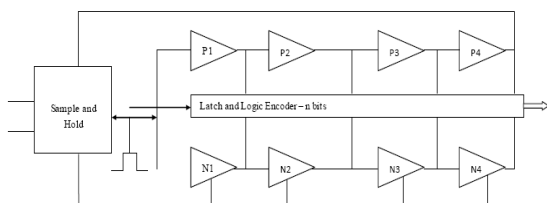


Fig 3 : Proposed delay line ADC

The basic structure consists of buffers and flip-flops. Initially, all buffers are reset to 0. Then, a rising edge is fed into the Start and propagates along the delay line. After a while, the Stop goes high and triggers the flip-flops to sample the delay line, which produces a thermometer code such as $1 \dots 1100 \dots 0$. The number of 1s in the codeword provides a measure of the delay between the Start and Stop, with a resolution of D , which is the delay per buffer. The delay line based ADC is designed in 250nm technology using T-Spice tool.

a) Sample and Hold circuit

We use a differential structure to achieve better linearity, in which two identical delay lines are controlled by differential voltages. Each conversion period has two phases: sampling phase and pulse propagation phase. In the sampling phase, S/H gets new samples, and the delay cells are reset. In the pulse propagation phase, the input rising edge propagates in the delay line at a speed determined by the sampled voltage. The S/H circuit shown in Fig.2.4 consists of the input switching network and differential inputs that convert the input voltage difference to differential voltages applied to the positive and negative delay lines. The bias point of the delay cell and the conversion gain (determined by R) are optimized for the highest possible linearity.

The input switching network marked by the dashed area is composed of two non-overlapping clock phases generated by the clock phase generator and samples the input differential signal. Devices Ms3 and Ms6 are dummies to reduce the common mode change caused by the charge injection of the switches. The sampled signal is converted to two differential current sources using the differential pair and the source degenerated resistor. The current is copied to all the delay cells producing the input dependent delay relation required for the delay line operation. M5 and M6 are current sources which determine the bias current. The current mirrors M3 and M4 are biased around the middle point in the delay cell swing.

The settling time of the sample and hold is extremely important and directly affects the effective number of bits. In order to get maximum number of bits the delay line time window (T_s) should be a significant part of the sampling time, so the remaining for the settling of the SHA is small. The time constant of the settling equals to $\tau = C_{load}/g_{mM1,M2}$. In signal processing, sampling is the reduction of a continuous signal to a discrete signal. A common example is the conversion of a sound wave (a continuous signal) to a sequence of samples (a discrete-time signal). A sample refers to a value or set of values at a point in time and/or space. A sampler is a subsystem or operation that extracts samples from a continuous signal. A theoretical ideal sampler produces samples equivalent to the instantaneous value of the continuous signal at the desired points. In electronics, a sample and hold circuit is an analog device that samples (captures, grabs) the voltage of a continuously varying

analog signal and holds (locks, freezes) its value at a constant level for a specified minimal period of time. Sample and hold circuits and related peak detectors are the elementary analog memory devices. They are typically used in analog-to-digital converters to eliminate variations in input signal that can corrupt the conversion process. The reasons for using such a circuit are varied. In some kinds of analog-to-digital converters, the input is often compared to a voltage generated internally from a digital-to-analog converter.

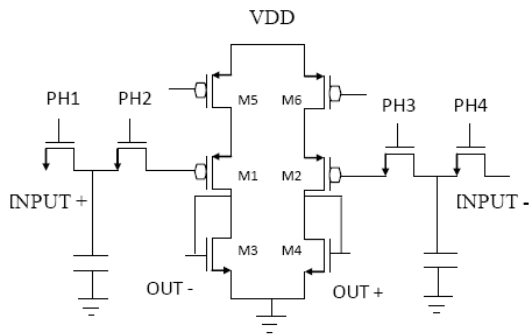


Fig 4 : Sample and Hold circuit

b) Delay Line Cell

The idea of delay amplification has been utilized traditionally for time-to-digital conversion with applications in phase locking and jitter measurements. The idea is to apply a pulse to a delay loop and measure the distance in terms of number of delay cells the signal passes in a certain amount of time. This number is proportional to the time window. There are also variations to this basic structure including using a variable delay and a constant time window. In ADC applications, the slope-based ADCs are well known as ADCs based on a delay depending on the input signal. These analog-to-digital conversions are based on a small variation in the delay and giving a sufficient amount of time. Their target is relatively high accuracy but slow sampling rates. In Fig.2.5, the concept of the quantization method is shown. A digital pulse is applied to a chain of delay cells and the pulse propagates in the chain. After a fixed time window (T_s) the pulse has propagated to some extent and the number of the delay cells is a measure of the amount of delay for each cell.

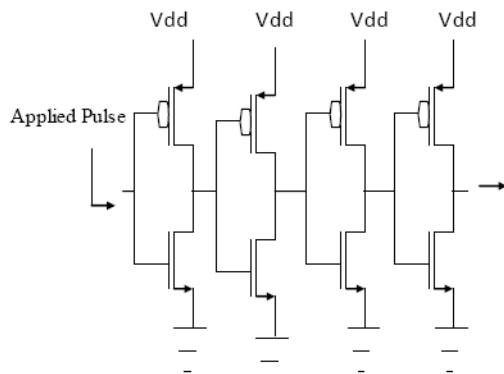


Fig 5 : Delay line cell

c) Voltage-to-time-to-digital ADCs

In light of the analogy between ADCs and TDCs, it seems promising to design new ADCs using similar structures. A straightforward way is the voltage-to-time-to-digital approach. The sampled input voltage V_{in} is first converted to a time window, which is then quantized by TDCs. This design stems from integrating ADCs, which are believed to be suitable for high-resolution applications. However, typical integrating ADCs quantize the time window by counting a reference clock, which largely constrains them to low-frequency applications. As digital delay-line-based TDCs can now achieve time resolutions on the order of picoseconds, they can achieve a much higher speed of AD conversion if used in place of counters.

d) Voltage-to-delay-to-digital ADCs

Another way of using delay lines in ADCs is the voltage-to-delay-to-digital scheme. The input signal modulates the delay per buffer instead of the time window, and thus, the number of delay cells the signal passes through in a constant time window is proportional to the input voltage. As an illustration, we will present an ADC simulated in 250-nm CMOS processes, which shows compatibility with technology scaling. A major advantage of the delay-line-based structure lies in its all-digital implementation, which makes it compatible with technology scaling. In addition, the delay-line structure introduces time-domain amplification into the design and potentially leads to better solutions. In particular, signal can be amplified in the time domain by simply extending the time window. This is particularly attractive to weak-signal acquisition.

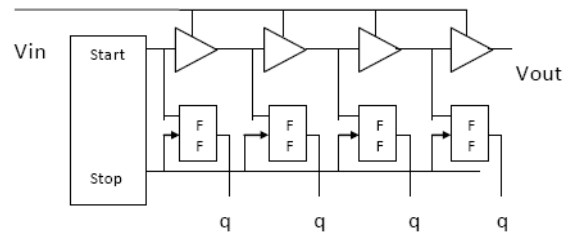


Fig 6 : Voltage-to-delay-to-digital ADC

IV. DELAY BASED ADC USING P AND N BLOCK (ENHANCED PROPOSED ADC)

The proposed delay ADC has a long delay line in both the upper and lower side. Since the delay line is too long, the time taken for the pulse to pass through it is high or the time window will be more than the required delay. To overcome this problem we are going for the enhanced delay line based ADC. The P and N block architecture which is shown above will be implemented instead of the delay line buffer. The CMOS logic structure of both P and N block is shown in Fig.4.2.

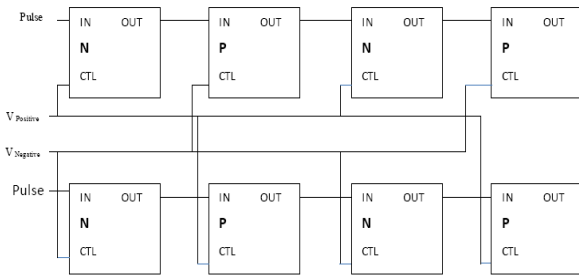
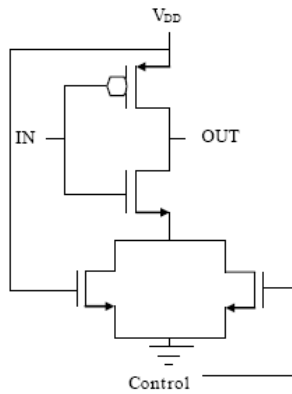


Fig 7: P and N block architecture

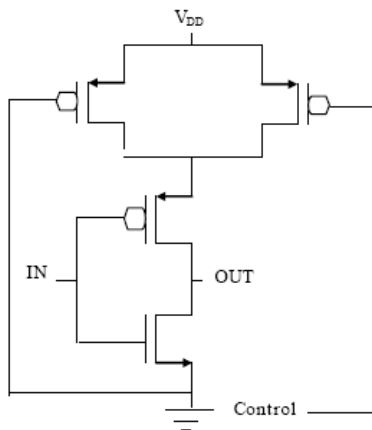
P And N Block Architecture

There is a control voltage in both the P and N block structure. The out+ and out- from the sample and hold circuit is given as the control voltage to this blocks. When the control voltage is high, the N block will act as an inverter and when the control voltage is low, the P block will act as an inverter. The power consumption of this enhanced ADC will be less when compared to the delay based ADC. The enhanced delay based ADC is designed in 250nm technology using T-Spice tool.



N BLOCK

Fig 8 : N Block



P BLOCK

Fig9 : P Block

V. SIMULATION RESULT

The SAR ADC and Delay Line Based ADC is designed and implemented in T-SPICE environment. The output waveforms for the above mentioned Architectures are obtained and shown below.

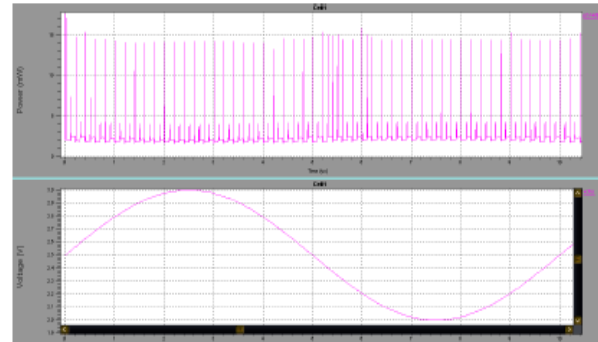


Fig 10 : Waveform of Power Consumption in SAR-ADC

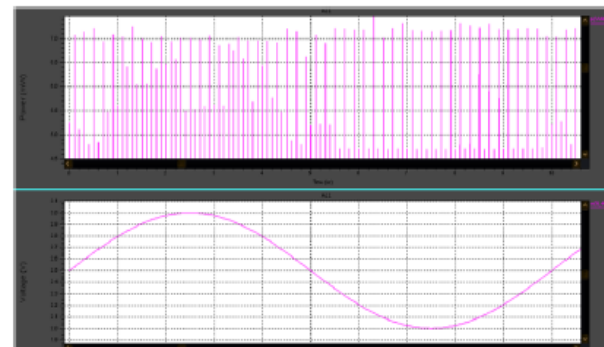


Fig 11: Waveform of Power Consumption in Delay Line Based ADC

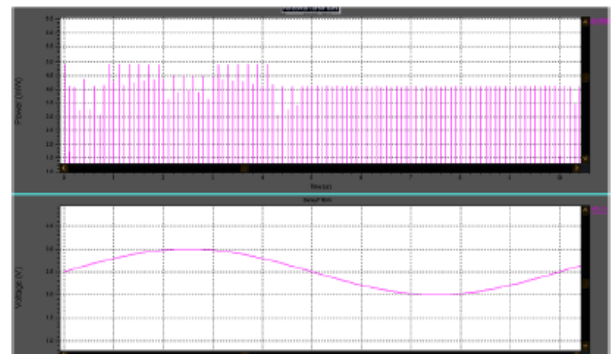


Fig 12: Waveform of Power Consumption in Delay Based ADC Using P & N Block

Performance Analysis

The Parameters such as Power consumption, Sampling frequency and Resolution for the Sar ADC and Delay based ADC are compared below.

ADC PARAMETERS	SAR ADC	DELAY LINE BASED ADC		DELAY LINE BASED ADC USING P AND N BLOCK	
Power(mW)	15.2	7.2	15	5	13.5
Sampling Frequency(Hz)	100M	500M	500M	1G	1G
Resolution	4-bit	4-bit	6-bit	4-bit	6-bit

Table 5.1 Comparison of Parameters

The Performance comparison of SAR ADC and Delay based ADC shows that the power consumed by Delay based ADC is half the power consumed by SAR ADC. Even with the increased bit resolution for a Delay based ADC, the power consumed is same as the SAR ADC. The power consumption of enhanced ADC with 6-bit resolution is further low compared to proposed ADC.

VI. CONCLUSIONS AND FUTURE WORK

A Delay line based ADC that is compatible with digital CMOS and high processing speed is designed and simulated in 250nm technology using T-Spice (Tanner). It also provides the freedom of amplifying signals in the time domain and will save the average power dissipation. This delay based converter is introduced for high-speed and low-power applications. The proposed structure is advantageous in deep-submicron technology compared to voltage-based data converters. Compared to threads the proposed ADC is more power efficient and compact. This design takes the full advantage of finer digital process migration, achieving low power consumption, high speed and very good scalability.

In Future, due to its purely digital core, the delay based ADC can be a good fit for applications which require a fast ADC with low number of bits in a small area. Typical applications might include an onboard ADC for a microcontroller where a digital CMOS technology is used. This could be used in a touch screen application. The division can be handled by the microcontroller or microprocessor resulting in a much smaller overall footprint for the ADC. The ability to integrate the ADC and a microcontroller could potentially reduce the overall system cost by reducing the total number of ICs

in the system. The designed delay line ADC can be easily scaled for higher sampling rates in Future.

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