BRIDGELESS BUCK PFC CONVERTER SIMULATION

Mir Aamir Shafi, Dhanalakshmi
M. Tech Student, Asst. Professor Department of Electrical Engineering, Dayananda Sagar College, Bangalore-78, India.
Email: aamir.shafi87@gmail.com, dhanalaxmisk@gmail.com

Abstract - In this paper, a bridgeless buck PFC converter further improves the low line efficiency of the buck front-end by reducing the conduction losses by reducing the number of semiconductor components. Conventional buck PFC correction rectifier have high conduction losses and low switching losses, so the conduction losses get reduced. The bridgeless buck rectifier also works as a voltage doubler. Although the output voltage is doubled, the switching losses of the primary switches of the dc/dc output stage are still lower than that of the boost power factor correction.

Keywords: Power Factor Correction, generators, Bridgeless rectification, Buck Converter, Conduction losses, switching losses

I. INTRODUCTION

Maintaining a high efficiency over an entire range (90-264) becomes a challenge for ac to dc converters that are used for power factor correction. There is also requirement of high power factor and low total harmonic distortion in the current drawn from the utility. Various topologies have been introduced in this respect for attaining high power factor and low harmonic distortion.

The boost topology was the widely used topology at the earlier stage. Conventional boost bridge PFC rectifier comprises of full bridge rectifier followed by a boost converter. This bridge arrangement has high conduction losses due to the number of semiconductor devices and hence the efficiency is less. Another drawback of the boost PFC was the relative high output voltage, this high voltage effects the switching losses of the primary switches of the downstream dc/dc output stage. To reduce this loss a bridgeless boost topology [3] was introduced which eliminates the use of bridge rectifier.

Even though boost PFC is efficient, the output voltage of boost converter is greater than the input which facilitates the use of higher rating semiconductor devices at the downstream. The drawback of universal line boost PFC front end can be overcome by implementing buck PFC topology [1]. This paper analyses the bridgeless buck converter which further improves the efficiency of the buck converter [2] by minimizing the number of simultaneously conducting devices. This converter also works as a voltage doubler circuit whose output voltage is twice the input voltage. Even though the output voltage is doubled the switching losses at the downstream is lower than the boost frontend.

The bridgeless PFC buck topology improves efficiency at low line of the universal line range than the bridgeless boost PFC rectifier.

II. BRIDGELESS PFC CIRCUIT

The bridgeless buck PFC circuit, as shown in Fig. 1. Here the two buck converters are connected back and they operate in alternative halves of the line-voltage cycle. During positive half-cycles of line voltage buck converter consisting of switch S1, diode D1, freewheeling diode D3, Inductor L1, Capacitor C1 operates. The voltage across C1 is regulated by pulse width modulation of the switch S1. During negative half cycle of the line voltage switch S2, freewheeling diode D2 and D4, inductor L2 and capacitor C2 operates. Here the output voltage across C2 is regulated by pulse width modulation of switch S2. The voltage available at the output resistor is the sum of the voltages across capacitors C1 & C2.

Since the output voltage of the bridgeless buck converter is the sum of voltage across two capacitors Vo = 2DVin
A. Positive half cycle

During positive half cycle the buck converter comprising of diode D1, switch S1, inductor L1, capacitor C1 and freewheeling diode D3 is operating. When switch S1 is on, the inductor L1 stores energy and the current path is through diode D1, switch, inductor L1, capacitor C1. When the switch is off the current freewheels through the diode D3. The voltage across the capacitor is regulated by the pulse width modulation of switch S1. The buck converter which is operating during positive half cycle is shown in bold lines.

B. Negative half cycle

During the negative half cycle the buck converter consisting of switch S2, diode D2, inductor L2, capacitor C2 and the freewheeling diode D3 operates. When the switch is on the inductor L2 stores energy and when the switch is off, the energy is discharged through the freewheeling diode D3. The output voltage of each buck converter is available across the capacitors. Since the direction of current is in the same direction in both the capacitors, the output voltage obtained across the load resistor is twice the voltage obtained at any of the buck converter. The buck converter operating during the negative half of the line voltage is shown in bold lines in the figure given below.

III. SIMULATION & RESULTS

Simulation of the bridgeless buck PFC converter is done in MATLAB and the results obtained are shown below. The PWM signal required for providing gate pulses to the switches of the buck converters are generated by comparing the ramp signal with the reference.

The input current and voltage is shown in fig. 5. The voltage across the two MOSFET switches S1 and S2 is shown in fig. 6.

Furthermore, the output dc voltage is shown in fig. 7. The PWM across the switches is shown in fig. 8.

Figure below shows the simulink model of the bridgeless buck converter with two inductors. It shows the closed loop simulation where in, the output is feed back to the input.
IV. CONCLUSION

In this paper a bridgeless buck PFC converter has been analysed. The bridgeless buck PFC converter consists of two buck converters connected back to back. Since the number of devices is less as compared to the bridge circuit, the conduction losses and the switching losses are less. The input current and voltages are nearly in phase that represents the high power factor.

REFERENCES


