Design and Comparison of Reversible and Irreversible Sequential Logic Circuits

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Abstract--- Reversible or information-lossless circuits have applications in digital signal processing, communication, computer graphics and cryptography. They are also a fundamental requirement in the emerging field of quantum computation. We investigate the synthesis of reversible circuits that employ a minimum number of gates and contain no redundant input-output line-pairs. It is not possible to realize quantum computing without implementation of reversible logic. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. A Fault tolerant reversible logic has gained importance as they consume low power and less heat dissipation. The benefits of logical reversibility can be gained only after employing physical reversibility. Every future technology will have to use reversible gates in order to reduce power. In this paper, we have designed RS flip flop, D flip flop by using reversible gate. The proposed designs are better than the existing proposed ones in terms of number of reversible gates and garbage outputs. So, this realization is more efficient and less costly than other realizations.

Index terms - Reversible logic, Reversible gate, Power dissipation, Flip-Flop, Garbage

I. INTRODUCTION

Energy loss is an important consideration in digital circuit design, also known as circuit synthesis. Part of the problem of energy dissipation is related to technological non- ideality of switches and materials. Higher levels of integration and the use of new fabrication processes have dramatically reduced the heat loss over the last decades. Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. It has wide applications in low power CMOS and Optical information processing, quantum computation and nanotechnology. Irreversible hardware computation results in energy dissipation due to information loss. According to Landauer research, the amount of energy dissipated for every irrepressible bit Operation is at least KTln2 joules, where $K = 1.3806505*10^{23} m^2 kg^2 K^1$ (joule/Kelvin^{-1}) is the Boltzmann's constant and T is the temperature at which operation is performed [1]. In 1973, Bennett showed that KTln2 energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs [2]. Energy dissipation can be reduced or even eliminated if computation becomes Information--lossless Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history.

II. THE CONCEPT

Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility. The benefits of logical reversibility can be gained only after employing physical reversibility. Physical reversibility is a process that dissipates no energy to heat. Absolutely perfect physical reversibility is practically unachievable. Computing systems give off heat when voltage levels change from positive to negative: bits from zero to one. Most of the energy needed to make that change is given off in the form of heat . Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minute amount of energy on each transition. Reversible computing strongly affects digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs. It will impact instruction sets and high-level programming languages as well. Eventually, these will also have to be reversible to provide optimal efficiency. In the design of reversible logic circuits the following points must be considered to achieve an optimized circuit.

They are

- Fan-out is not permitted.
- Loops or feedbacks are not permitted
- Garbage outputs must be minimum
- Minimum delay
- Minimum quantum cost.

III. NEED OF REVERSIBLE COMPUTING

Reversible computing provide Reliable and low power design, high performance circuits synchronous with speed and processing power. Reversible circuits that conserve information, by uncomputing bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance. It again Improve computational efficiency this can be done by building circuits which reduce energy from state will save energy. Reversible computing will also lead to improvement in energy efficiency. It Increase portability of device to reduce element size to atomic size. It has incurred more hardware cost, but power cost and performance are dominant than hardware cost. Hence need of reversible computing cannot be ignored in computing era.

IV. FAULT TOLERENT REVERSIBLE LOGIC GATES

Fault tolerance enables a system to continue its operations correctly when an error occurs in some parts of it. Parity checking is one of the widely used mechanisms for detecting single level fault in Communication and many other systems. It is believed that if the parity of the input data is maintained throughout the computation, no intermediate checking would be required [5-6]. Therefore, parity preserving reversible circuits will be the future design trends towards the development of fault tolerant reversible systems in nano technology. A gating network will be parity preserving if its individual gates are parity preserving [5]. Thus, we need parity preserving reversible logic gates to construct parity preserving reversible circuits [3][4]. Parity checking is one of the oldest, as well as one of the most widely used, methods for error detection in digital systems.

IV. REVERSIBLE LOGIC GATES

A reversible logic gate has equal number of input and output terminals and there is one to one mapping between them. again we can say, gate is reversible if we can determine input vector from output vector and vice-versa. Reversible gate should practically loose very little amount of energy. Fan-out is not allowed in reversible circuits however fan-out can be achieved using additional gate. In this paper we have discuss basic reversible gate like Feynman gate, Fredkin gate, NFT gate, NEW gate, Peres gate, R gate, Toffoli gate and URG gate. Which we have used in implementing reversible sequential circuits.

A. Feynman gate

Feynman gate is a 2*2 one through reversible gate

as shown in figure l[8]. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A B. Quantum cost of a Feynman gate is l. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

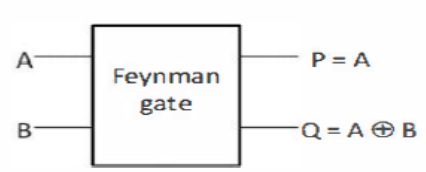


Figure 1: Feynman gate

B. Fredkin Gate

Figure 3 shows a 3*3 Fredkin gate[8]. The input vector is I (A, B, C) and the output vector is 0 (P, Q, R). The output is defined by P=A, Q=A'B EB AC and R=A'C EB AB. Quantum cost of a Fredkin gate is 5.

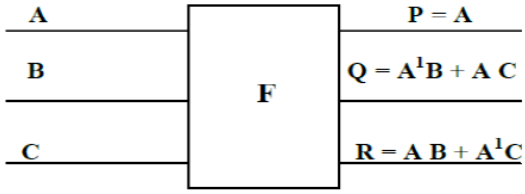


Figure 2:Fredkin gate

C. Peres Gate

The three inputs and three outputs i.e., 3*3 reversible gate having inputs (A, B, C) mapping to outputs (P = A, Q = A B, R = (A.B) C). Since it requires 2 V+, 1 V and 1 CNOT gate, it has the Quantum cost of 4. The Peres gate is shown in the Figure 3.[7-8]

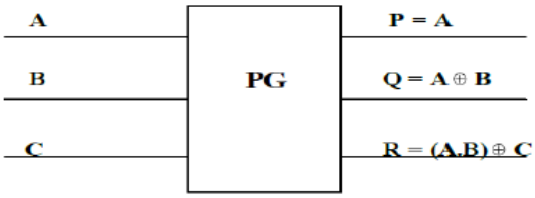


Figure 3:Peres gate

D. Toffoli-Gate

The 3*3 Reversible gate with three inputs and three outputs[8]. The inputs (A, B, C) mapped to the outputs (P=A, Q=B, R=A.B C) is as shown in the Figure4[8].

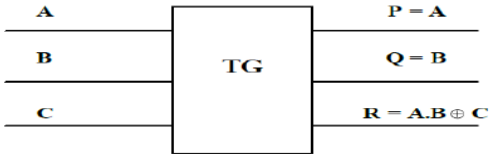


Figure 4:Toffoli gate

E. NFT Gate

The 3*3 Reversible gate with three inputs and three outputs[8]. NFT stands for Novel Fault Tolerant Gate. The inputs (A, B, C) mapped to the outputs (P=A^B, Q=BC`^AC`, R=BC^AC`) is as shown in Figure 5.

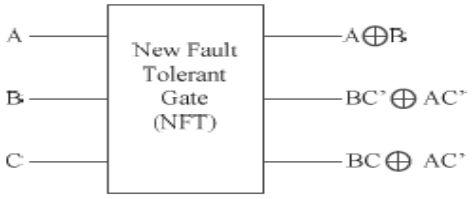


Figure 5: NFT gate

F. NEW Gate

The 3*3 Reversible gate with three inputs and three outputs[8]. The inputs(A,B,C) mapped to the outputs(P=A, Q=A`B^C, R=A`C`^B`) is as shown in Figure 6.

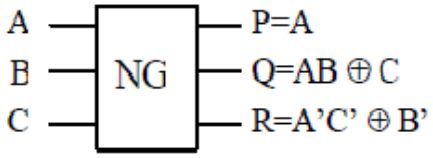


Figure 6: NEW gate

G. URG Gate

The 3*3 Reversible gate with three inputs and three outputs. URG stands for Universal Reversible Gate. The inputs(A,B,C) mapped to the outputs (P=(A+B)^C, Q=B, R=AB^C) is as shown in Figure7

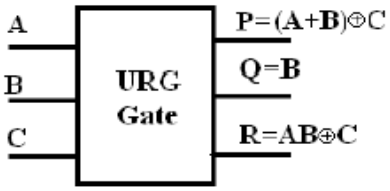


Figure 7: URG gate

H. DKG Gate

A 4* 4 reversible DKG gate that can work singly as a reversible Full adder and a reversible Full subtractor. If input A=0, the proposed gate works as a reversible Full adder, and if input A=1, then it works as a reversible Full subtractor.[9]. DKG gate is shown in figure 8.

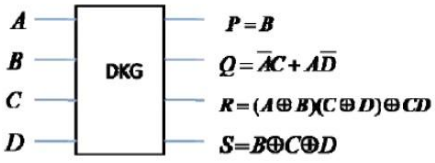


Figure 8:DKG gate

The power consumed by the above given reversible gates based on Cadence encounter® RTL compiler is given in Table A.

Gate	Leakage power(nw)	Dynamic power(nw)	Total power(nw)
BJN	6.643	123.966	130.609
DFY	1.377	202.276	212.643
FEYN	5.188	96.026	101.212
FRED	10.741	170.852	181.593
MCL	2.458	64.212	66.67
NEW	12.783	267.697	280.48
NFT	12.403	260.718	273.183
PERES	11.365	235.533	246.893
R	11.332	234.688	246.02
TOFF	6.177	139.507	145.684
URG	17.079	324.428	341.307

Table A

V. SEQUENTIAL CIRCUITS

In a sequential circuit the output at a given time is dependent on the input at that time as well as on the earlier inputs. Thus, the earlier input sequence needs to be stored, there by sequential circuits always have a memory associated with them. The operation of a sequential circuits is expressed in terms of states. The state or internal state is a set of signals at a given points in a sequential circuits.

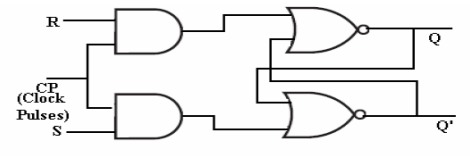
Sequential circuits are classified broadly into synchronous sequential circuits and asynchronous sequential circuits. Synchronous sequential circuits are controlled by a master clock. The input to the circuit is sampled at discrete instances of these clock pulses which determines the circuit operation. Thus, sequential circuits change state as well as their outputs at specific clock instances. The operation of asynchronous circuits are not controlled by any clock pulses. The outputs respond immediately to a change in input. The basic memory elements in sequential circuits is the Flip-Flops. A Flip-Flop is a sequential circuit which can store 1 or 0 indefinitely.

VI. DESIGN OF SR FLIP-FLOP

In SR Flip-Flop there are Three inputs and two output as shown in Table1. One of the input is a clock. If this clock is in high state(logic 1), the state of output will change. If Clock is at low state(logic 0), output remains in previous state. Other two inputs are S and R. If these both are in low states, outputs remain in previous state. The outputs of remaining possible inputs is shown in Table I. This Flip-Flop gives a forbidden state when both the inputs are at logic 1.

TABLE I
TRUTH TABLE OF SR FLIP-FLOP

CLK	S	R	Qnext	Comment
⎍	0	0	Q	hold previous state
⎍	1	0	1	set
⎍	0	1	0	reset
⎍	1	1	N/A	forbidden
—	X	X	Q	hold previous state



SR flipflop designed using Reversible logic gates like Toffoli gate, R gate, URG gate, NEW gate, Peres gate, Fredkin gate and NFT gate. The last two belong to fault tolerant gates.

There are two methods in designing the flip flops, one is by building basic gates and replacing the irreversible basic gates. Second using expression obtained from truth table. But for building SR flipflop, the first method is more suitable which gives less garbage outputs than the second method. SR flipflop using second method is very difficult to build the flipflop because of forbidden state in SR flipflop, even it is built we would get more garbage outputs. The following figures will explain better.

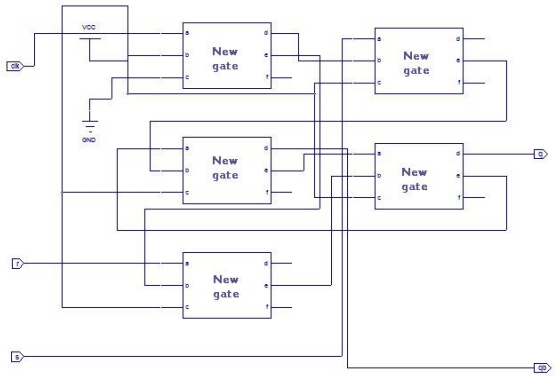


Fig 9. SR flipflop using NEW gate

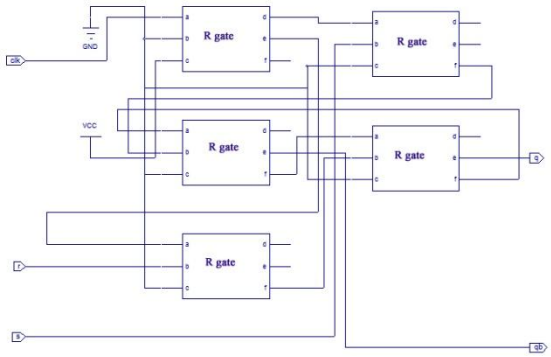


Fig 10. SR flipflop using R gate

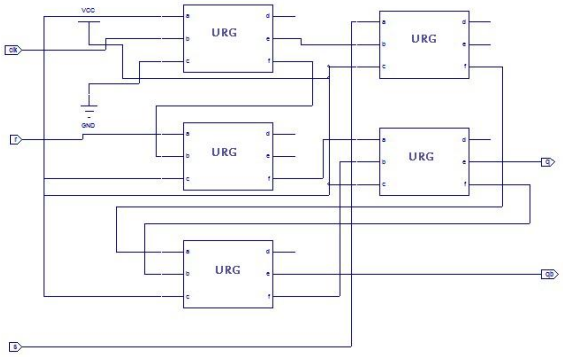


Fig 11. SR flipflop using URG gate

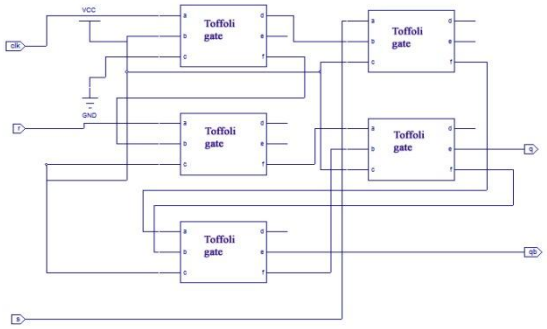


Fig 12. SR flipflop using Toffoli gate

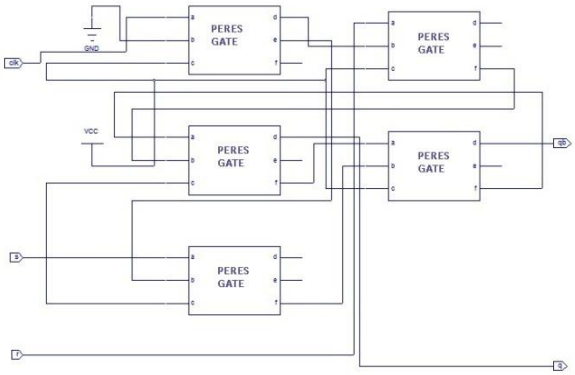


Fig 13. SR Flip-flop using Peres gate

Above designs are minimized in number of gates and garbage outputs compared to the designs in literature[10]. Table Ia gives comparison between proposed and literature design.

Gate used to design SR flipflop	Garbage output	Number of gates
NEW gate	7	5
R gate	7	5
URG gate	7	5
Toffoli gate	7	5
Peres gate	7	5
Already Proposed	8	6

Table Ia

Design of SR flipflop using fault tolerant reversible gates which are useful in parity preserving between inputs and outputs is shown in figure 13 and 14.

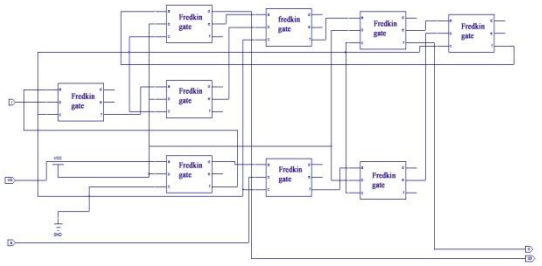


Fig 14. SR flipflop using Fredkin gate

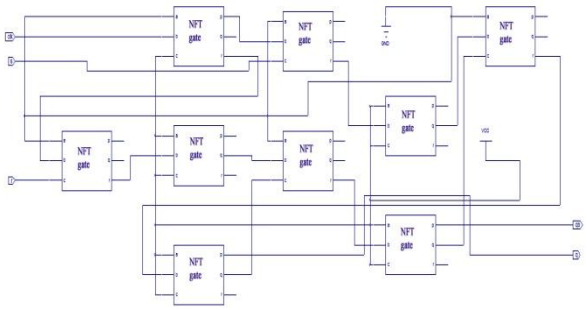


Fig 15. SR flipflop using NFT gate

Gate used to design SR flipflop	Garbage output	Number of gates
Fredkin gate	15	9
NFT gate	15	9
Already Proposed	None in literature	None in literature

Table Ib

Table Ib gives the number of gates and garbage outputs in SR flipflop built using fault tolerant reversible gates. From table Ib we can conclude that, using above mentioned fault tolerant gates will give more garbage outputs compared to other reversible gates.

Now let us compare the power consumed by the flipflop in both reversible and irreversible gates. Table Ic gives the power consumption of SR flipflop using different reversible gates and irreversible gate.

Gate	Cell	Leakage power (nw)	Dynamic power (nw)	Total power (nw)
SRFF	9	27.204	449.213	476.417
SRFFTOFF	5	9.657	193.546	203.203
SRFFRED	9	20.999	351.574	372.573
SRFFNFT	9	24.579	407.194	431.773
SRFFR	5	9.658	193.543	202.200
SRFFPERES	5	9.657	193.546	203.203
SRFFNEW	5	9.657	193.546	203.203
SRFFURG	5	9.657	193.546	203.203

Table Ic

SRFF is irreversible SR flipflop, SRFFTOFF is flipflop using Toffoli gate, SRFFRED is flipflop using Fredkin gate, SRFFNFT is flipflop using NFT gate, SRFFR is flipflop using R gate, SRFFPERES is flipflop using Peres gate, SRFFNEW is flipflop using NEW gate, SRFFURG is flipflop using URG gate.

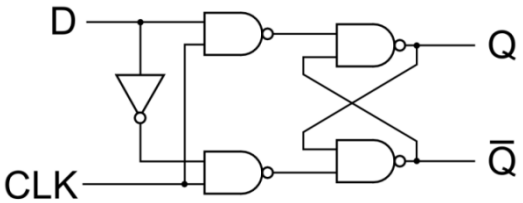
From table Ic we have proved that reversible gate consumes less power compared to irreversible gates.

VII. DESIGN OF D FLIPFLOP

In D Flip-Flop there are Two inputs and two output as shown in Table II. One of the input is a clock. If this clock is in high state(logic 1), the state of output will change. If Clock is at low state(logic 0), output remains in previous state. Other input is data_in. The outputs of remaining possible inputs is shown in Table II.

TABLE II
TRUTH TABLE OF D FLIP-FLOP

CLK	D	Q_{next}	Comment
⎍	0	0	reset
⎍	1	1	set
⎽	X	Q	hold previous state



D flipflop designed using Reversible logic gates like Toffoli gate, R gate, URG gate, NEW gate, Peres gate, Fredkin gate and NFT gate. The last two belong to fault tolerant gates. In the design D flipflop we have used the two methods which have mentioned earlier. By using the expression obtained from truth table garbage outputs can be reduced. Which is a prime factor of reversible logic. The following figure explains the design of D flipflop.

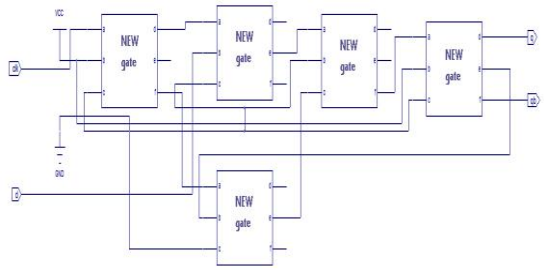


Fig 16. D flipflop using NEW gate

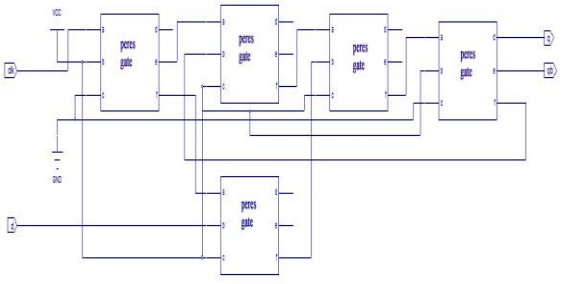


Fig 17. D flipflop using Peres gate

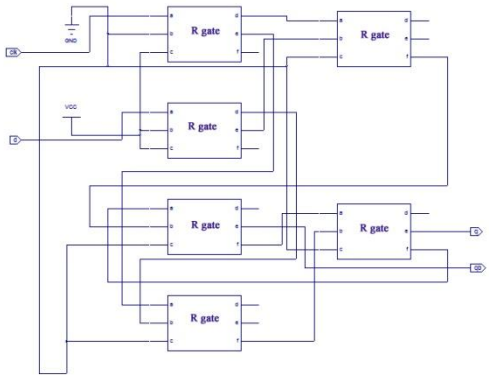


Fig 18. D flipflop using R gate

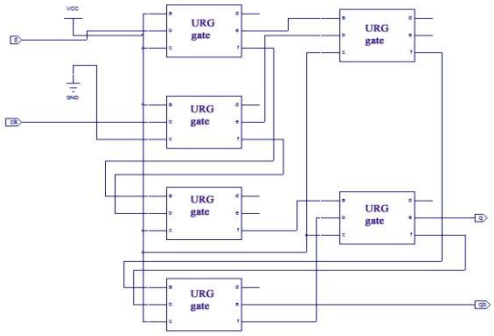


Fig 19. D flipflop using URG gate

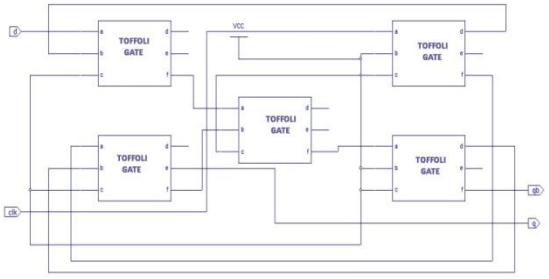


Fig 20. D flipflop using Toffoli gate

All above designs are minimized in number of gates and garbage outputs compared to the designs in literature[10]. Table IIa gives comparison between proposed and literature design.

Gate used to design D flipflop	Garbage output	Number of gates
NEW gate	7	5
R gate	8	6
URG gate	8	6
Toffoli gate	7	5
Peres	7	5
Already Proposed	8	7

Table IIa

Design of D flipflop using fault tolerant reversible gates which are useful in parity preserving between inputs and outputs is shown in figure 19 and 20. Even in D flipflop design fault tolerant flip flops have resulted in more garbage output. Figure 19 and 20 depict this.

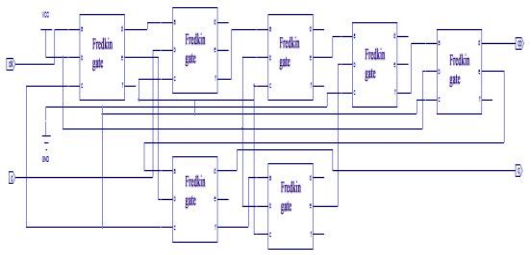


Fig 21. D flip flop using Fredkin gate

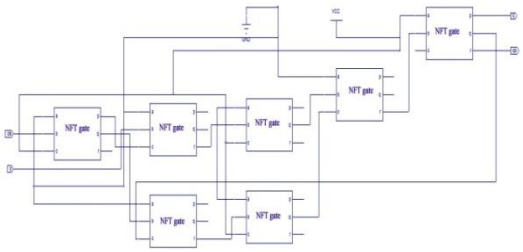


Fig 22. D flip flop using NFT gate

Gate used to design D flipflop	Garbage output	Number of gates
Fredkin gate	11	7
NFT gate	11	7
Already Proposed	None in literature	None in literature

Table IIb

Table IIb gives the number of gates and garbage outputs in D flip flop built using fault tolerant reversible gates. From table IIb we can conclude that, using above mentioned fault tolerant gates will give more garbage outputs compared to other reversible gates.

Now let us compare the power consumed by the flip flop in both reversible and irreversible gates. Table IIc gives the power consumption of D flipflop using different reversible gates and irreversible gate.

Gates	cell	Leakage power (nw)	Dynamic power (nw)	Total power (nw)
IRDFF	8	26.827	423.263	450.090
DFFTOF	6	11.112	205.571	216.683
DFFRED	8	21.705	328.982	350.687
DFFNFT	8	21.705	328.982	350.687
DFFR	6	11.112	205.570	216.682
DFFPERES	6	11.112	205.571	216.683
DFFNEW	6	13.193	226.769	239.962
DFFURG	6	11.112	205.571	216.683

Table IIc

IRDFF is irreversible SR flipflop, DFFTOFF is flipflop using Toffoli gate, DFFRED is flipflop using Fredkin gate, DFFNFT is flipflop using NFT gate, DFFR is flipflop using R gate, DFFPERES is flipflop using Peres gate, DFFNEW is flipflop using NEW gate, DFFURG is flipflop using URG gate.

From table IIc we have proved that reversible gate consumes less power compared to irreversible gates.

VIII. CONCLUSION

Reversible circuits is an emerging technology with a promising application. In the last decade synthesis of reversible circuits has extensively been studied, an impressive accomplishment have been made. The proposed reversible design is utilized for efficiently designing RS and D flip flop. As, flip flops are most important memory elements used in several circuits like RAM, Logic blocks of FPGA. We have compared our design with existing designs and we have minimized the garbage outputs and number of gates. The proposed design is highly optimized. Thus, the resulting sequential circuit is most efficient.

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