FINFET: A Supplement to MOSFET in semiconductor Industry Beyond 22nm

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Abstract- As nanometer process technologies have advanced, chip density and operating frequency have increased, making power consumption in battery-operated portable devices a major concern. Even for non-portable devices, power consumption is important because of the increased packaging and cooling costs as well as potential reliability problems. Thus, the main design goal for VLSI (very-large-scale integration) designers is to meet performance requirements within a power budget. Therefore, power efficiency has assumed increased importance. This paper explores FinFETs (fin-type field-effect transistors), an emerging transistor technology that is likely to supplement or supplant bulk CMOS (complementary metal-oxide-semiconductor) at 22-nm and beyond, offer interesting delay–power tradeoffs. Simulations are done using PADRE simulator.

Keywords: Scaling, tradeoff, short-channel effects, FINFETS.

I. INTRODUCTION

The silicon metal-oxide-semiconductor field effect transistor (MOSFET) is one of the most important devices in the semiconductor industry. the MOSFET has been incorporated in monolithic integrated circuits (ICs) to serve as a basic switching element for digital logic and as an amplifying device for analog applications. While the basic planar structure of the MOSFET has remained mostly unchanged, its size has been shrunk by many orders of magnitude over the past thirty years. The trend showing an exponentially increasing number of transistors on a chip was first predicted in 1965 and has since come to be known as 'Moore's Law'. Device scaling has enabled IC chips to operate faster and with greater functionality each new technology generation.

The enhanced speed and complexity of IC chips has been accompanied by an increase in power dissipation. Fig. 1.1 depicts the evolution of power density as the gate length is scaled. The active power arises due to the dissipative switching of charge between the transistor gates and supply/ground terminals during logic operations. The sub-threshold power, also known as static or standby power, is dissipated even in the absence of any switching operation. It arises due to the fact that the MOS transistor is not a perfect switch; there is some leakage current that flows through it in the off-state.

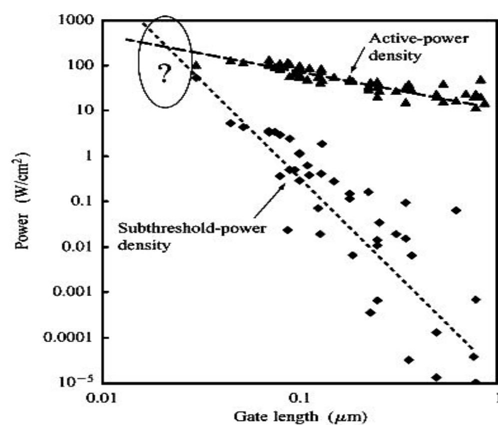

Fig. 1.1 Active and standby power density trends plotted from industry

While the active power density has steadily increased with gate length scaling, the static power density has grown at a much faster rate. The latter was a relatively insignificant component of power just a few generations back, but it is now comparable in magnitude to the active power. Management and suppression of static power is one of the major challenges to continued gate length reduction for higher switching speed. The double-gate (DG) FET(FINFET) is a promising device structure that can potentially replace conventional transistors in future technology generations.

II. FIN FET

The FINFET(DGFET) is a novel device structure that is a promising candidate for replacing conventional bulk MOSFETs beyond the 45-nm technology node. Fig.2.1 shows a schematic cross section of this device. The DG FET can be regarded as an evolution of the regular MOSFET structure, with a second gate placed below a thin body in which the channels are formed. In the most effective FIN FET implementation, both gates are electrically connected (driven by the same voltage), and the top and bottom gate dielectrics have the same thickness. This is known as a symmetric FINFET. The main advantage of placing the second gate is the increased electrostatic gate control over the channel. The

two gates are more effective at shielding the drain electric field lines so as to prevent them from reaching towards the source and degrading the short channel effects. In addition, by removing part of the bulk substrate and replacing it with a gate, one eliminates sub-surface current leakage paths that are far away from gate control. As a result of the better electrostatics, the FINFET is scalable to shorter gate lengths than bulk FETs. Since the two gates and thin body are sufficient to suppress short channel effects, the body is left undoped. This improves channel carrier transport due to increased mobility resulting from reduced ionized impurity scattering and lower vertical electric field. In addition, the undoped body is more immune to discrete dopant fluctuation effects.

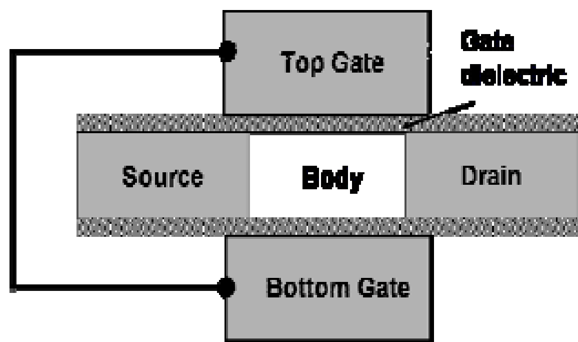

Fig. 2.1 Schematic of a symmetric FINFET

For effective suppression of short channel effects, the silicon body between the two gates must be made very thin (typically, it should be less than half of the gate length). Achieving a uniform and controllably ultrathin body is one of the key requirements for a FINFET from an intrinsic scalability viewpoint

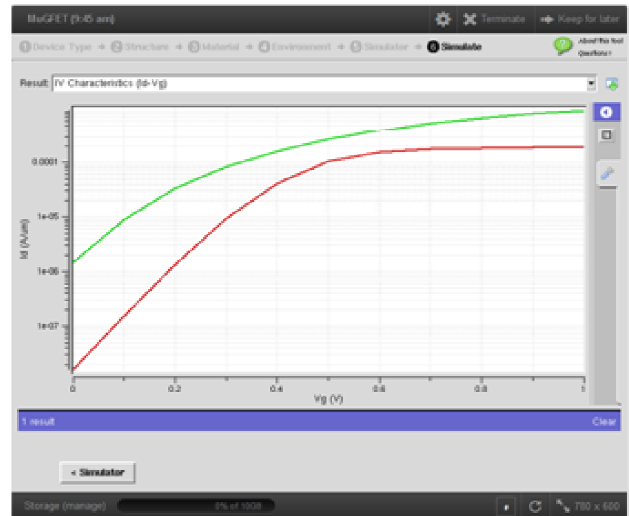

Fig 2.2: Simulation waveform of FINFET

III. CONCLUSION

FinFETs are a promising substitute for bulk CMOS for meeting the challenges being posed by the scaling of conventional MOSFETs. Simulation results show that FINFET offers better performance than MOSFET beyond 22nm.

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