Simulation and Verification of Digital Delay based Instantaneous Frequency Measurement Technique for Electronic Warfare receivers

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Abstract—The Instantaneous Frequency Measurement (IFM) receiver is employed to intercept and measure the frequency of intercepted radar signal instantaneously for Electronic Support purpose. The IFM receiver uses delay lines to compare the phase of the input signal to measure the frequency. This paper outlines the concept of Digital delay based IFM technique to measure the frequency of received signal that replaces the physical delay in the conventional IFM receiver technique by introducing time delay through sampling the RF signal. The theoretical background of the technique is followed by MATLAB simulation results. The verification of the algorithm is carried out through the real time data from 90^0 hybrid, sampled and interfaced to FPGA.

Key words: Electronic Support, IFM (Instantaneous Frequency Measurement), Digital delay, IQ hybrid.

I. INTRODUCTION

The IFM receiver is employed to intercept and measure the frequency of intercepted radar signal instantaneously for Electronic Support purpose [1]. The conventional IFM technique [2-4] uses physical delay lines of length greater than the reference delay line to obtain a phase difference between the original signal and the delayed version of the signal. The two signals (i.e., the original signal and the delayed signal) are passed through a phase correlator to generate the sine and cosine values of the obtained phase difference. By processing these signals in a simple DIFM processor, we get the frequency of the intercepted signal. The IFM receiver is popular in an EW system because of its wide input band, accurate frequency reading, and simple structure.

The Digital Delay based IFM technique (DDIFM) uses a digital delay that replaces the physical delay lines in the conventional IFM technique. With the advent of Analog-to-Digital Converter (ADC) with high sampling frequency of several Giga-Sample-Per-Second (GSPS),high input RF input bandwidth and high dynamic range, it is possible to replace the physical delay lines with digital delay, facilitating realization of a compact lightweight IFM receiver.

II. CONVENTIONAL IFM TECHNIQUE

The Conventional IFM technique is shown in Fig.1 [5]. The RF signal generator generates an RF signal of frequency 'f'. This after amplifying is passed through a power divider whose two outputs are fed to a phase correlator through RF cables. These RF cables are differed by a length of 'L' where the shorter is considered to be reference cable and longer is said to be a delay line of length 'L'. This extra length 'L' causes a phase difference of βL given by

$$\beta L = \left(\frac{2\pi}{\lambda}\right) L = \left(\frac{2\pi f\sqrt{\varepsilon_r}}{c}\right) L \text{ Radians} \qquad (1)$$

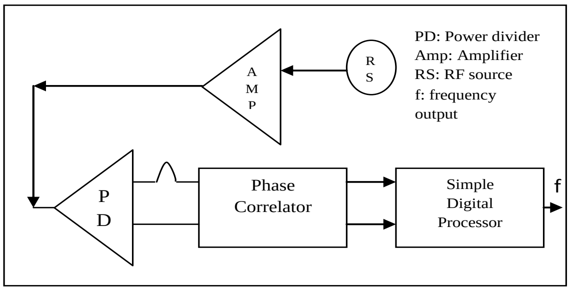

Fig.1. Conventional delay line technique using one delay line.

The phase correlator is a device that takes two inputs with a phase difference of βL and provides DC output of X = cos (βL) and Y = sin (βL). A simple digital signal processor does the phase-to-frequency operation of

$$f = \frac{c \tan^{-1}\left(Y/_X\right)}{2\pi L\sqrt{\varepsilon_r}} \qquad (2)$$

to measure the frequency from the two outputs obtained from the phase correlator. Considering as modulo-2π-wrapped, in the above equation, it can be derived that the unambiguous bandwidth is BW and is given by

$$BW|_{U,GHz} = \frac{300}{L_{mm}} \qquad (3)$$

and an error in frequency measurement is

$$f_{err} \;\alpha\; \frac{\text{function}(X,Y)}{L} \qquad (4)$$

i.e. function of phase-correlator nonlinearity which is ~ 10–15º in the frequency range of 0.5–2 GHz and delay line length.

As f_{err} is inversely proportional to L, so longer the delay line length, higher is the frequency measurement accuracy. But at the same time, band width is also inversely proportional to L. So longer delay line length results in lower bandwidth of operation. Hence for a required band width, if the delay line used is longer than that specified, it results in phase ambiguity (in turn frequency ambiguity). This shows that IFM with single physical delay line is not adequate to provide high accuracy and wide bandwidth at the same time. Hence there is a necessity to use multiple delay lines, as shown in Fig. 2, where longest delay line is used to provide fine frequency accuracy and shorter delay lines are used to resolve the ambiguities to get wide bandwidth of operation. It is to be noted here that DIFM processing which includes ambiguity resolution and also phase-to-frequency conversion, is not as simple as one using one delay line.

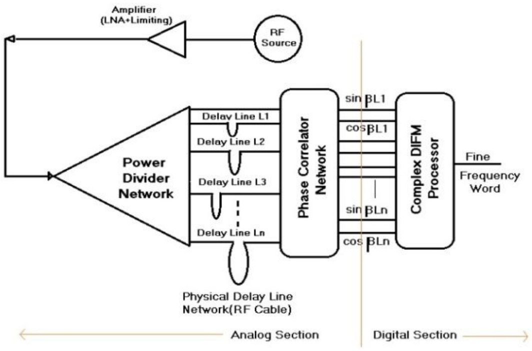

Fig.2. Fine DIFM using Multiple Delay Lines

III. CONCEPT OF DIGITAL DELAY BASED IFM TECHNIQUE

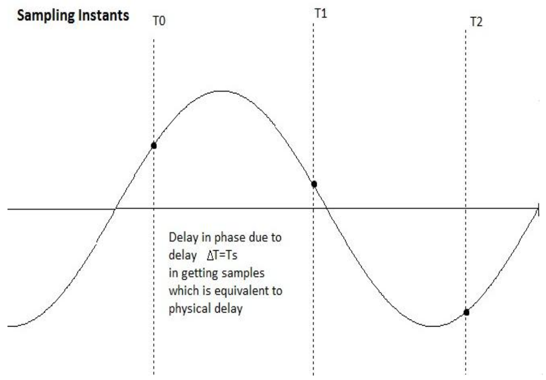

Fig.3. Digital delay based IFM sampling concept.

The phase of the signal (let's say, a sinusoidal signal) is a function of its frequency. Hence, the phase of the signal can be used to find the frequency. In the case of digital delay based IFM technique, RF signal is not physically delayed but instead, sequences of delayed absolute phase of a RF signal are obtained by introducing time delay by sampling the RF signal at certain interval ($T = T_s$) as shown in Fig. 3.

The differential phase between the samples (T_1 & T_0), (T_2 & T_0), (T_3 & T_0) and so on till (T_N & T_0) is obtained by subtracting the absolute phases at those particular instants. The differential phase between time-instants [T_1 & T_0], [T_2 & T_0], up to [T_N & T_0], can be derived by subtracting the absolute phase of the reference signal at those instants. To get the modulo-360° wrapped absolute phase (i.e. unambiguous over 0 to 360°) of the RF signal, only one signal is not sufficient as only sinusoid or co-sinusoid is unambiguous over 180° whereas arc-tangent operation over both sinusoidal and co-sinusoid provides modulo-360° -wrapped absolute phase as shown in Fig 4. This modulo-360° -wrapped phase can be unwrapped [6] to find its actual value which will be discussed further.

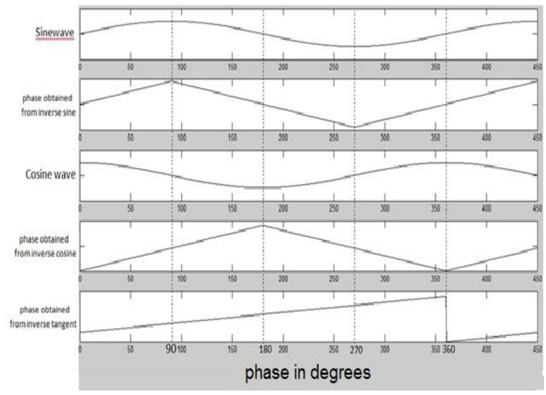

Fig.4. Necessity of I-Q sampling to get unambiguous absolute phase over 0 to 360°.

The phases at the samples are selected such that the ratio between them is known. Once we get the differential phase, the following step is to resolve the phase ambiguity. This ambiguity can be resolved by using the known ratio of the phases. For example, if we take the ratio of 2, then the phase at the second sample is twice that of the first one. By using this we can unwrap the phase at second sample. The corrected phase at second sample is used to unwrap the phase of the next sample. This can be continued for phases of further samples.

Then the phase - to - frequency conversion operation is performed same as the conventional method. Here the error in the frequency measured (f_{err}) is given as

$$f_{err} \ \alpha \ \frac{\text{function}(I,Q)}{\text{Digital delay}} \qquad (5)$$

which is dependent on amplitude & phase imbalance in IQ Hybrid and 'Digital Delay' is a function of NT_s. Hence frequency accuracy increases with the increase in 'digital time delay' (i.e. NT_s, neither N nor T_s alone) but at the cost of pulse handling capability. So in the case of Digital Delay based IFM (DDIFM), variable frequency accuracy (depending on the available pulse width) can be implemented with ease without incorporating any hardware change. Whereas in the case of conventional IFM, this is possible only after incorporating more number of physical delay lines which is usually not feasible due to hardware constraints.

In this technique, minimum possible time delay is nothing but sampling period i.e. Ts or equivalently physical delay

$$L_{min,mm} = 300 \times T_{s,ns} \qquad (6)$$

Hence, from relation in Eqn (3), theoretical unambiguous bandwidth can be derived as

$$BW|_{U,GHz} = \frac{1}{T_{s,ns}} = F_{s,GHz} \qquad (7)$$

But due to limited input RF 3dB-BW handling capability of ADC, the practical unambiguous bandwidth = minimum [sampling frequency, 3dB input RF BW] of ADC [7]. Some of the important characteristics of Frequency Receivers [8] are:

1) Sensitivity
2) Dynamic Range
3) Throughput Time
4) Accuracy
5) Probability of Intercept.

Several research groups reported the work in this area on the characteristics of IFM receivers [9-13]. In this paper, an attempt has been made to reduce the RMS error in order to improve the frequency accuracy.

IV. FLOW CHART FOR DDIFM ALGORITHM

The following Fig.5 shows the detailed flow chart of the algorithm discussed in the above section. Hardware realization of the DDIFM technique, Verification and MATLAB simulation results have been discussed in the next section.

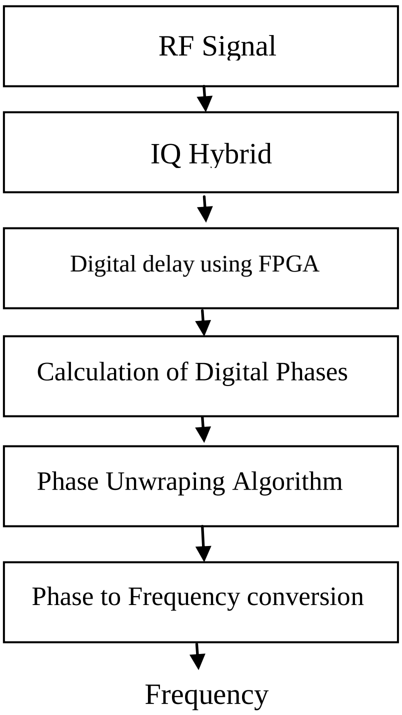

Fig. 5. The flow chart for DDIFM algorithm

V. DISCUSSION OF SIMULATION RESULTS

To implement DDIFM algorithm the following specifications have been considered.

1) Input frequency is taken as intermediate frequency range of the RF signal i.e., from 750MHz – 1250MHz.
2) The power level of the signal is selected in the range of 0 dBm to -40 dBm.
3) The error RMS is acceptable up to 1MHz.

With the specifications given above, the algorithm has been implemented in MATLAB. To verify that the algorithm works in every condition, the algorithm is simulated and tested for the following cases and are discussed in the following sub sessions.

1) With I and Q signals without any error i.e., pure I and Q signals.
2) A phase error is introduced with the signals.
3) Taking real time samples from chip scope Pro.
4) Forming cluster of phases to enhance accuracy.

V.A Simulation Results With Pure I And Q Signal

Firstly, the experiments are carried out on pure signals i.e., the signals are noise free. A co-sinusoidal signal (I) is taken and its quadrature phase shifted signal i.e., a sinusoidal signal (Q). Both the signals are sampled at an equal sampling rate and synchronized sampling has to be done. The frequency taken is in the intermediate frequency range of the RF signal i.e., from 750MHz – 1250MHz and signal is sampled with a sampling frequency of "Fs = 625MHz". From the phases at all samples, differential phases are calculated and are as shown in Fig.6.

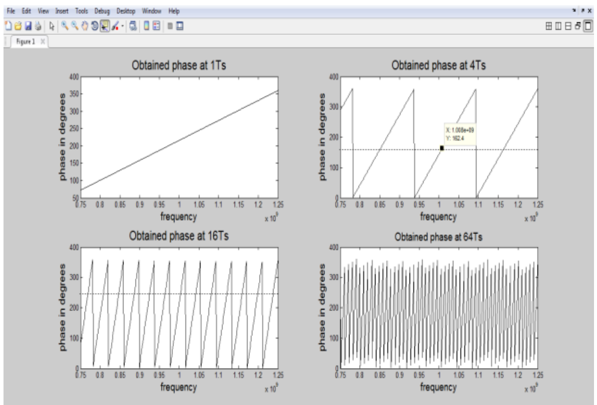

Fig. 6. Phase differences obtained with pure I and Q Signals

From the Fig.6, it can be observed that the phase with $4T_s$ time difference is ambiguous over the taken frequency range. This is because the phase is modulo-360°-wrapped. Therefore, when the phase to frequency conversion is done there will be an ambiguity between the frequencies that produce same phase value, over the horizontal line drawn in Fig.6. To remove this ambiguity and produce the frequency unambiguous over the taken frequency range, the ϕ_1 (phase with $1T_s$ time difference), ϕ_4 (phase with $4T_s$ time difference), ϕ_{16} (phase with $16T_s$ time difference), ϕ_{64} (phase with $64T_s$ time difference), phases have to be unwrapped. To maintain a clarity of the phases, the sampling frequency is selected such that it produces an unambiguous phase at ϕ_1, so that the ϕ_4, ϕ_{16}, ϕ_{64} phases can be unwrapped using ϕ_1. After correction of ϕ_4, ϕ_4 is used to un-wrap ϕ_{16}, ϕ_{16} is used to un-wrap ϕ_{64} and so on. The obtained actual phase values of ϕ_1, ϕ_4, ϕ_{16}, ϕ_{64} are represented as actual phase at 1Ts, actual phase at 4Ts, actual phase at 16Ts and actual phase at 64Ts respectively and are shown in Fig.7. The frequency of the signal is taken on X-axis and phase in degrees is taken on Y-axis.

From the Fig.7, it can be observed that all the actual values of the ϕ_1, ϕ_4, ϕ_{16}, ϕ_{64} phases are now increasing with increase in frequency. Therefore, there is no ambiguity in the phase to frequency conversion. Now the phase-to-frequency conversion operation is performed by using the Eqn (8).

$$\text{frequency} = \frac{\text{actual\_phase} * f_s}{360 * \text{sample\_time}} \quad (8)$$

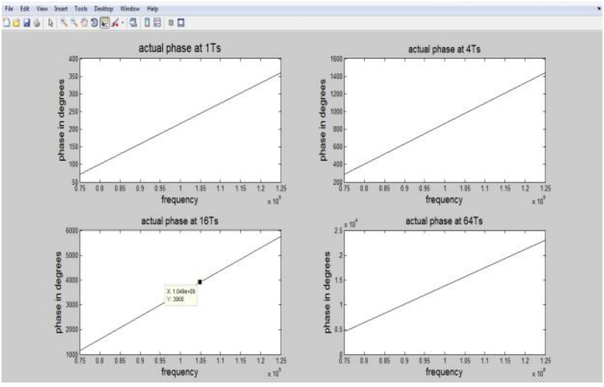

Fig. 7. Actual Phases obtained with different sampling time differences (i.e. $1T_s$,$4T_s$,$16T_s$,$64T_s$)

The frequencies obtained are shown in Fig.8.

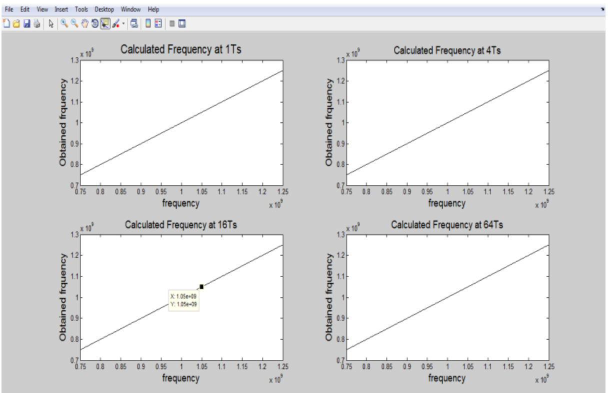

Fig.8. Obtained frequencies from actual phase values

In graph plotted, the display of the reading is shown on the tag, on the calculated frequency at $16T_s$. It can be observed that the X-axis reading i.e., input frequency and the Y-axis reading i.e., output calculated frequencies are equal. It means that the input frequency is exactly replicated at the output without any error.

V.B Simulation Results By Introducing Phase Error With I And Q Signals

One can doubt that when frequency can be obtained at the $1T_s$ level itself, then why to go for higher sampling times i.e., for $4T_s$, for $16T_s$ and so on. As stated in the above section, if there is no error in the obtained phase, there will be no error in the calculated frequency. But one cannot expect everything goes on like a bright sunny day. There is a possibility that error can occur in the obtained phase because of the following reasons:

1) I-Q hybrid introduces an error because of its imbalances.

2) The quantization error present in the signals after sampling.

3) I signal and Q signal are taken from different cables and may have some phase difference.

4) Due to various hardware factors.

All these contribute to the overall error in the ϕ_1, ϕ_4, ϕ_{16}, ϕ_{64} phases. If an error occurs in the obtained phase, then from the Eqn (8), it can be said that the calculated frequency at $1T_s$ has more error compared to the calculated frequency at $16T_s$ or of more sampling time. It is because from the Eqn (8), it can be observed that the phase is divided by the sampling time. Hence, it can be noted that if there is an error in phase and sampling time is more the calculated frequency is more accurate. For example, if there is an error of 'e' degree in phase at $1T_s$ time difference the frequency obtained will be

$$\text{frequency} = \frac{(\text{actual\_phase} + e) * f_s}{360 * (1Ts)} \quad (9)$$

But at $16T_s$ time difference the frequency obtained will be

$$\text{frequency} = \frac{(\text{actual\_phase} + e) * f_s}{360 * (16Ts)} \quad (10)$$

Hence, the obtained frequency from Eqn (10) is more accurate than from Eqn (9).From the above description it is clear, why to go for higher sampling times but the question is how much error in phase, the algorithm supports. To know this the following set of equations are used to calculate the maximum error that can be allowed in phase. If

$$\Psi_1 = \phi_1 + 2\pi m_1 \quad (11)$$

$$\Psi_4 = \phi_4 + 2\pi m_4 \quad (12)$$

Where 'Ψ_1' is the actual phase at $1T_s$ and m_1 is the number of cycles the signal has completed before the sample is taken. 'Ψ_4' is the actual phase at $4T_s$ and m_4 is the number of cycles the signal has completed before the sample is taken. As the ratio taken is 4.

$$\frac{\Psi_1}{\Psi_4} = 4 \qquad (13)$$

$$4(\phi_1 + 2\pi m_1) = (\phi_4 + 2\pi m_4) \qquad (14)$$

$$\frac{4\phi_1 - \phi_4}{2\pi} = m_4 - 4m_1 \qquad (15)$$

Since m_1 and m_4 are always integers their difference is also an integer. If there is an $+\Delta$ error in ϕ_1 and $-\Delta$ in ϕ_4 then

$$\frac{4\Delta + \Delta}{2\pi} < 0.5 \qquad (16)$$

From the above equation it can be said that the error 'Δ' should be less than 36°. Therefore, a random error of less than 30° is introduced in the phase calculated from the pure signals and the algorithm is executed. The phase obtained is as shown in Fig.9.

From these phases actual phases are calculated and are as shown in Fig.10. From the Fig.10, it can be observed that as mentioned earlier the error in the phase value seems to be less at higher sampling time.

The phase-to-Frequency conversion is done and the obtained frequencies are as shown in Fig.11 and it can be observed that higher accuracy is obtained higher sampling times.

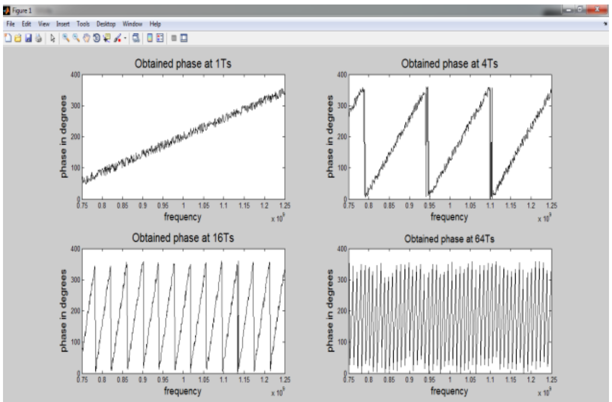

Fig.9. Obtained phases by introducing an error in phase

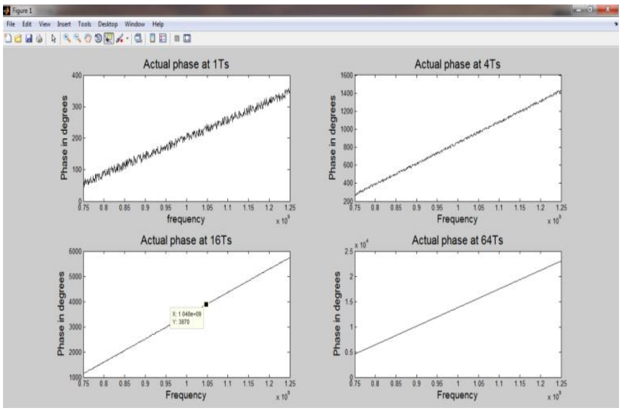

Fig.10. Obtained actual phases by introducing an error in phase

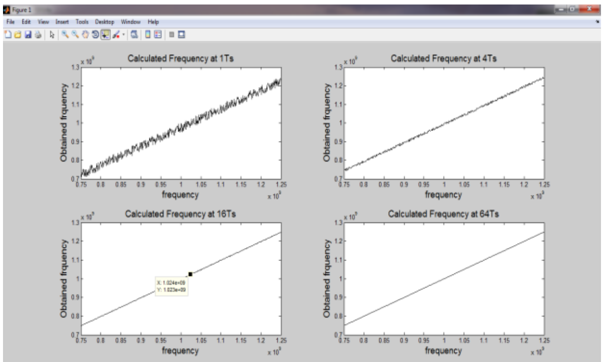

Fig.11. Obtained Frequency by introducing an error in phase

The algorithm is simulated several times by introducing random error values in the obtained phases and the error in calculated frequency is measured by the Eqn (17).

$$RMS = \frac{\sqrt{\text{sum of } (f_{original} - f_{calculated})^2}}{\text{number of times calculated}} \qquad (17)$$

In Fig.12, the number of times the code is simulated is taken on X-axis and error in frequency is taken on Y-axis. It may be observed that the error in frequency is 1.97MHz. The accuracy may be further improved by forming clusters of phases which will be explained in section-VII.

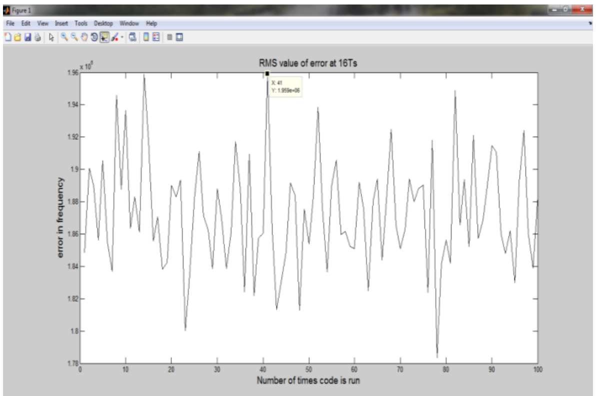

Fig.12. Error in obtained frequency by introducing an error in phase

V.C Verification through Real Time Data From ChipScope Pro

The intermediate frequency range of the RF signal i.e., from 750MHz – 1250MHz is taken and is passed through the IQ hybrid. This gives two outputs of which one is in-phase signal (I) and the other is quadrature phase signal (Q).

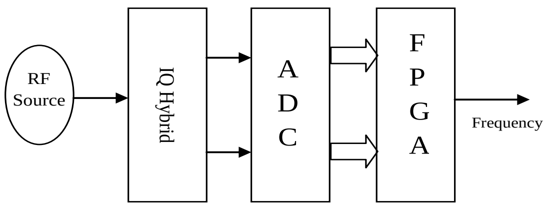

Fig.13. Block diagram of hardware realization of DDIFM technique.

These I and Q signals are then sampled by an ADC and the output of ADC is passed to the targeted FPGA which contains the algorithm coded in it. The whole setup is as shown in the Fig.13. The output of the 90° hybrid for the frequency of 1250MHz is as shown in Fig.14. The X-axis in the plot represents time and the Y-axis represents amplitude for a frequency of 1250MHz. The leading signal is the I signal and the lagging signal represents the Q signal. This signal is then converted to a bit file i.e. binary data format using the tool named Chip Scope Pro and the samples collected are as shown in Fig.15 and this data is tested with the MATLAB Simulation.

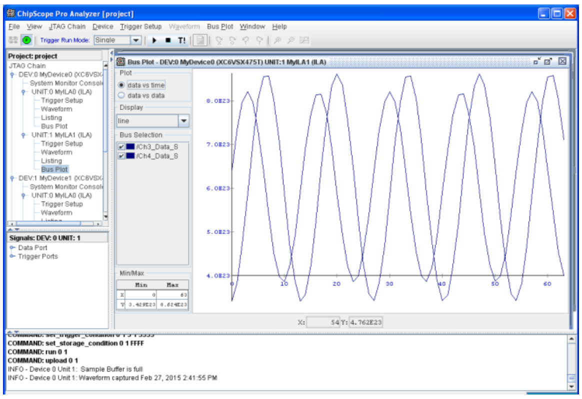

Fig.14. Output of hybrid at 1250 MHz

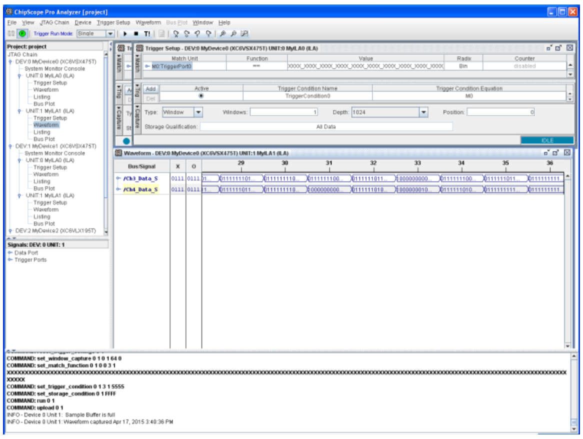

Fig.15. IQ Hybrid output at 1250 MHz from Chip Scope Pro

V.D Forming clusters of phases for improvement of accuracy

The samples collected are of sample size 10 bits per sample. These are now extracted in MATLAB and algorithm is simulated for the data collected at different frequencies and of different power levels. It is observed that at lower power levels the algorithm does not yield good results. Hence, to obtain good accuracy the phases are taken as average of the phases in the cluster of phases formed by taking differential phase between all samples with required time difference.

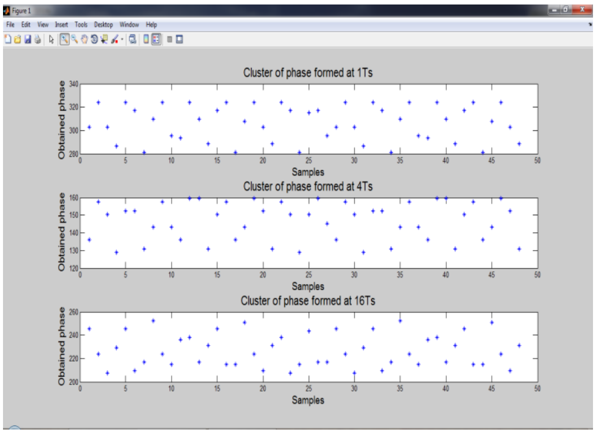

Fig.16. Cluster of phases formed at different sampling time differences

With this taking of average the error in phase gets minimized and the RMS value in the error in calculated frequency gets reduced and is less than 1MHz. As this is obtained at 16T_s itself, it does not need to go till 64T_s and more sampling times. This is also limited by the memory in the used FPGA and the levels to be taken i.e., for reaching 16T_s with a ratio of 4, it takes two levels of unwrapping phase at 4T_s and 16T_s where as for reaching 64T_s with same ratio of 4, it takes three levels of unwrapping phase at 4T_s,16T_s and 64T_s. Hence, it has to be chosen according to the requirement.

The algorithm is now simulated with the collected real time data and the frequency output obtained at 1250 MHz is as shown in Fig.17.The symbol '*' in Fig.17 is the output sample obtained.

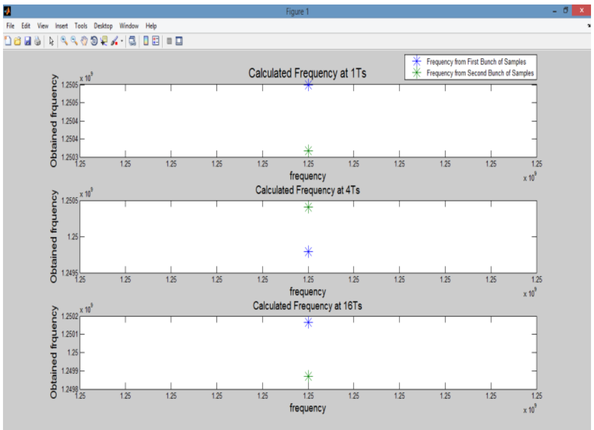

Fig.17. Frequency output at 1250 MHz of -10dBm power

This is simulated for different power levels of the input signal from 0 dBm to -40 dBm and the output frequency that is calculated is found to be less than 1MHz.

VI. OPTIMIZATION OF ALGORITHM

By seeing how much less size of the sample can be taken without compromising on the specifications of the system, the algorithm can be optimized. This can be done by extracting the samples as less in size i.e., the number of bits per sample has to be reduced. By reducing one bit at a time, it is found that algorithm is giving satisfactory results till sample size is 6. As more information is concentrated in the MSB part of the sample, the LSBs can be ignored. The following are the advantages when the number of bits per sample is reduced.

1) Computation complexity reduces.

2) Reduces the dynamic power consumption.

3) Reduces the area.

4) Increases the speed to some extent.

To represent the phase value also, only 6 bits are taken. Hence to represent the value of 0-2π radians, 3 bits are taken to represent integer part of the phase and 3 bits are taken to represent decimal part of the phase.

When only 3 bits are taken to represent the phase after the decimal point, the maximum phase that can be represented is only 0.875°. All the combinations of the three bit binary representation and the values have been calculated. The extra value in the phase that needs more bits is rounded off to the values that have been calculated. By doing so, the error in the resultant phase obtained is not more than 0.125°. This less error does not affect the algorithm and hence is acceptable. The frequency output obtained after optimizing the algorithm is as shown in Fig.18.

From the Fig.18, It may be observed that the error in calculated frequency at 6 bits per sample is slightly more or equal to the calculated frequency at 10 bits per sample. But the error in frequency does not cross the margin of getting the RMS value of the error of less than 1MHz.

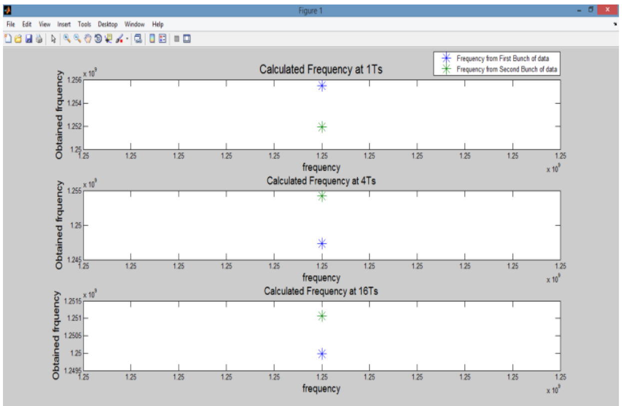

Fig.18. Frequency output at 1250 MHz of -10 dBm power after optimization

VII. CONCLUSION

Digital Delay based IFM technique has been implemented successfully. Simulation work is carried out using MATLAB to measure the instantaneous frequency of the unknown received signal. The initial MATLAB code gives a frequency accuracy with an RMS error less than 1.97 MHz. The MATLAB code is optimized by forming clusters of phases to achieve an accuracy with RMS error less than 1 MHz. To verify the simulation results in the hardware, optimized code is written in VHDL and ported on to Virtex-6 FPGA using ISE Design Suite. Real time samples from Chip Scope Pro are used to verify the algorithm and frequency accuracy with an RMS error of less than 1MHz has been achieved. The DDIFM is implemented using 10 bit ADC with 40 dBm dynamic range. However, the same frequency accuracy can be achieved by making use of 6 bit ADC with reduced dynamic range.

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