I. INTRODUCTION

Low-power is one of the most important targets of embedded system designs. Furthermore, low power implies lower cost of operation and smaller battery size to make applications more mobile. Embedded systems are used everywhere in today’s life and its demanding day by day. More productivity, less time to market are necessary for the product success. Most of the embedded products are battery operated, including portable data terminals handheld gaming consoles, media players, portable medical diagnostic equipments, smart watches, communications hot spots, battery-backed home and building automation navigation system, test and measurement devices, mobile robots, smart displays and many more. Furthermore, with increasing facilities of embedded system its complexity is also increasing. For low power consumptions there are several techniques like power supply gating, clock gating, Multi-switching (multi-Vt) threshold transistors, Multi-supply multi voltage (MSMV), Power gating with or without state retention, Substrate biasing, Dynamic voltage and frequency scaling (DVFS). But for optimized result DVFS technique is used over other techniques. At the system level, power and consumption can be defined as the sum of the following:

Total power consumed = Active mode power + standby(sleep)mode power.

Active power is calculated by summing dynamic power consumption and static power consumption. Dynamic power is calculated during the switching of transistors which depends on the clock frequency and switching activity. It also consists of switching power and internal power. In static power, transistor leakage current that flows whenever power is applied to the device. Static power is independent of the clock frequency or switching activity. Active power is given by PActive:

\[ P_{\text{Active}} = I_{\text{Leakage}}V + C_{\text{eff}} V_f \]

Where static power consumption is given by ILeakageV and dynamic power consumption is given by CeffV 2f.

To achieve power reduction, DVFS and DPM techniques are applied. In DVFS technique, component voltage and frequency are varied based on the system workload and runtime factors. In DPM, it selectively turns off the system components when they are idle. Also implementation of fault tolerance techniques such as standby sparing, “2out of 2” hardware redundancy with voter can be done.

II. LITERATURE REVIEW

For low power management, hardware platform is implemented in [1] where DVFS and DPM techniques are used with fault tolerance requirements. In this paper, hardware platform is implemented on the COTS devices (commercial off-the-shelf). This platform is designed for ARM-based microcontrollers, as this concept is general. Other embedded processors can be used in the design of this platform. This platform can be customized for any embedded system application.

Embedded systems are highly time-constraint. For hard real time execution, embedded system should be fault-tolerant and also satisfy its timing constraints. The use of hardware redundancy techniques for real-time systems is necessary when high reliability is the primary concern as hardware redundancy can increase the energy consumption[2]. In this paper, hardware redundancy techniques are implemented based on standby sparing with low power consumption.
In DPM, system switches dynamically between high-and low-consumption system power modes based on activity. In this paper, dynamic power management technique is used for multi-core based embedded mobile devices. The parallel programming paradigm like OpenMP have a property of explicitly indicating a region that should be parallelized[3].

In this paper, comparative studies of embedded systems are done for industrial application. This paper introduces comparative study of various implementation platform including microcontrollers, microprocessors, FPGAs, DPSs and ASICs. Examples of real-life designs decisions specific to development of such systems are presented[4].

In this paper, a solution to the problem of the obsolescence of digital parts in critical applications is obtained. This methodology is implemented using Field Programmable Gate Arrays. This system proposes a design flow which provides tools that makes the system more reliable. It performs a static analysis, dynamic analysis and protection processes which gives optimum solution of resources that reduces the area and performance overhead[5].

III. PROPOSED PLAN

In the proposed system, DPM and DVFS techniques are used for power management. Many of the embedded processors either do not have DVFS or apply DVFS only to the processor core[1]. So we are providing DVFS capability for microcontrollers including not only processors but also PLL, memory and I/O. In the previous work, the generalized concept of low power managements based on the COTS devices is implemented. To implement this concept we are customizing it to specific application. The smart library assistant device is designed on which all the techniques are applied and results will be tested. DPM and DVFS techniques are simultaneously implemented as they gives more power saving. DVFS is also used in executing parallel tasks; a two processor system consume less energy as compared with a single processor system[1]. This platform can also be used to implement fault tolerance techniques such as result checking, error detection mechanism or to check whether task is executed properly or not.

This platform is consist of the host computer, programmable power supply, two ARM-based microcontrollers, power measurement unit and debugging unit. With the use of programmable power supply, microcontroller dynamically set the voltages of the peripherals and the processor core pins. Proposed technique can be used to provide scalable voltages for the “Smart library assistant device”, as its supply voltage can vary in its operating range. In processing unit two ARM-based microcontrollers are used. Power management unit consist of a resistor placed between each microcontroller power and supply pins, the voltage drop across the resistor is measured and power is calculated.

Fig.2. Design flow of proposed work

IV. CONCLUSION

In this system, we propose a platform for energy management techniques and fault tolerance techniques for multiprocessor embedded system. This system is equipped with separate controllable variable voltages which are given to each microcontroller. By using DVFS and DPM techniques minimum power consumption can be achieved for “Smart library assistant device”. The platform is also equipped with power measurement unit, debugging unit and facilities for experimenting with different fault tolerance techniques. Although this platform is general and can be designed for any COTS devices and embedded processors.

V. REFERENCES


