# DSB-SC AM based Software Defined Radio (SDR) Design.

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**Abstract - The rapid growth in speed and density of programmable logic devices such as FPGA's (Field Programmable Gate Arrays) facilitates ever more complex designs to be build within a short time frame. The adjustability of a programmable device makes it easy to integrate a design with variety of peripherals or components on a single chip and makes it versatile. Implementation of a highly realized and efficient programmable digital DSB-SC (Double Side Band Suppressed Carrier) AM (Amplitude Modulation) modem on ARTIX-7 FPGA has been done for mastering towards the Software Defined Radio (SDR) application. Since DSB-SC is an analog modulation scheme, carrying out it in the digital domain introduces new challenges. The goal of this paper is to make out simulation and implement DSB-SC scheme on FPGA. Since FPGA is well suited for real time algorithms we choose it as platform for implementation. MATLAB R2012a is used for simulating the DSB-SC modulation and demodulation algorithms, and ARTIX-7 FPGA is used as implementation platform with Xilinx ISE 14.7 System Generator. The output waveforms are displayed and approved using Xilinx Chip Scope Pro.**

**Index Terms— ARTIX-7 FPGA, DSB-SC, SDR, MATLAB R2012a, SYSTEM GENERATOR**

## I. INTRODUCTION

Software defined radio (SDR) is a rising communication technology which can be applied in enhancement of hardware and can make progress of the various functions. Various modulation and demodulation technologies have became a core of the software defined radio (SDR) systems. In Software define Defined Radio (SDR) platform the components are implemented using software instead of implementing on the hardware. This project determines the design and implementation of Double Side Band Suppressed Carrier (DSB-SC) which is a Amplitude modulation technique used towards targeting the SDRs. Modulation is a process in which certain parameters of the baseband signal are varied in accordance with the carrier signal. Since DSB-SC is an amplitude modulation scheme the amplitude of the message signal can be varied with respect to the carrier signal. DSB-SC AM is carried out simply by multiplying a message signal with a carrier signal while the demodulation process is carried out with the help of a Phase Locked Loop (PLL) based Costas Loop which provides carrier synchronization and carrier recovery. Even though various FPGAs have been used for SDR implementations, ARTIX-7 FPGA is the good among all as it consumes very low power compared to other FPGAs and hence increases the efficiency of the overall design.

The model based design environment MATLAB/ Simulink is used to build a required design with the help of available predefined IP cores and leads to an automatic code generation in Hardware Description Language called VHDL. This code is implemented on FPGA for the real time output of the DSB-SC modulation and Demodulation. Section II of the paper gives detailed overview about the DSB_SC technique working and how it is modulated and demodulated.

## II. DETAILED VIEW OF DSB-SC AM TECHNIQUE.

Modulation and Demodulation of the DSB-SC technique is carried out with help of a modulating (message) signal m(t), and carrier signal C(t).following figure shows how to obtain both the modulated and demodulated signal.

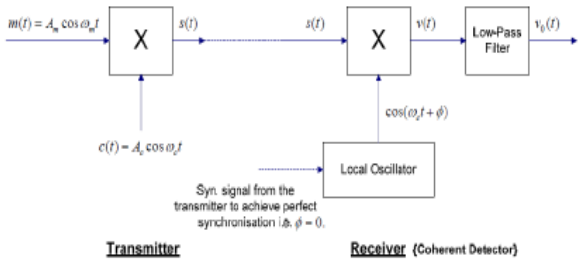


Fig1: DSB-SC Transmitter and Receiver

DSB-SC MODULATION

Modulation of a DSB-SC is carried out by multiplying a message (modulating) signal with a carrier signal having higher frequency than that of a modulating signal. The frequencies generated by the modulation are uniformly placed above and below the carrier frequency and carrier level is reduces to lowest practical level. Unlike in Amplitude Modulation (AM) DSB-SC do not transmit a wave carrier signal and much of the power is distributed among the upper and lower side bands there by increasing the power efficiency to 100%.

$$S(t) = c(t).m(t)$$

$$= A_c \cos(W_c t) \cdot A_m \cos(W_m t)$$

$$= A_c A_m \cos(W_c t) \cdot \cos(W_m t)$$

$$S(t) = A_c A_m/2 \cos(W_c+W_m)t + A_c A_m/2 \cos(W_c-W_m)t.$$

DSB-SC DEMODULATION

The message signal m (t) may be recovered from a DSB-SC modulated wave S(t) with a locally generated sinusoidal wave that has the same carrier frequency as the previous one.

$$V(t) = S(t) \cdot \cos(W_c t)$$

$$V(t) = [A_c A_m/2 \cos(W_c+W_m)t + A_c A_m/2 \cos(W_c-W_m)t].\cos(W_c t)$$

$$= A_c A_m/2 [\cos(W_c+W_m)t.\cos(W_c t) + \cos(W_c-W_m)t .\cos(W_c t)]$$

$$= A_c A_m/2 .1/2 [\cos(W_c+W_m+Wc)t + \cos(W_c+W_m-Wc)t +$$

$$\cos(W_c-W_m-Wc)t + \cos(W_c-W_m-Wc)t]$$

$$= A_c A_m/4[\cos(2W_c+W_m)t+\cos(W_m)t+\cos(2W_c+W_m)t+\cos(W_m)t].$$

The higher frequency components ($2W_c+W_m$) and ($2W_c-W_m$) are filtered out upon passing V(t) through the low pass filter and leaving behind the modulated signal.

$$V(0) = A_c A_m/2 \cos(W_m)t.$$

Since we cannot implement this basic demodulation method on hardware, a PLL based Costas loop is used for recovering the carrier which demodulates the modulated signal to get original message signal.

COSTAS LOOP FOR CARRIER RECOVERY.

A Costas loop is a kind of Phase Locked Loop (PLL) used to recover a message signal by transforming a carrier modulated signal into its complex envelope form. The received signal is transformed into its pre-envelope form and then multiplied by a complex exponential to form the complex envelope. Costas loop provides two path for carrying signal called as I (In phase) and Q (Quadrature) channels. Phase detector, loop filter, and Voltage Controlled Oscillator (VCO) are the basic building blocks of the Costas Loop. The purpose of the loop is to phase-lock the input modulated signal with local reference signal and to estimate the phase error between these two signals to demodulate the signal, and provide the data output. I channel multiplies input with VCO's output and Q channel multiplies input with the $90^0$ phase shifted VCO's output and passed through the low pass filters. The output of both the filters are multiplied again to get an error signal which is passed through the loop filter and provided as control input to the VCO in order to control phase and frequency of the VCO.

Consider a second order PLL based Costas Loop as shown in fig (2) to demonstrate the working of the system. The phase detector implements a complex multiplier which multiplies modulated signal and the complex VCO outputs to form real and imaginary parts for Q and I channels. Loop filter is designed with loop filter coefficients k1 and k2, and VCO is implemented by Direct Digital Synthesizer (DDS) which has a phase accumulator and a ROM look up table.

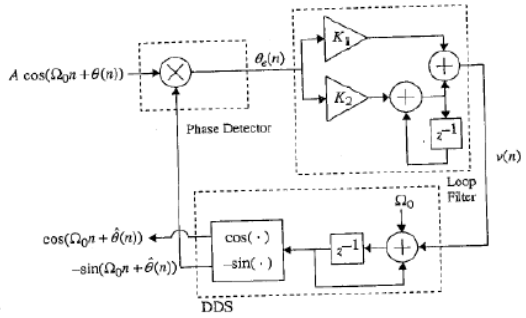


Fig2: Second order Costas Loop

The DDS provides two in phase quadrature waves

$$y_c(n) = \cos\left(\Omega_0 n + \hat{\theta}(n)\right)$$

$$y_s(n) = -\sin\left(\Omega_0 n + \hat{\theta}(n)\right).$$

Phase detector forms the product as shown below

$$x(n)y_s(n) = -A\cos(\Omega_0 n + \theta(n))\sin\left(\Omega_0 n + \hat{\theta}(n)\right)$$

$$= \frac{A}{2}\sin\left(\theta(n) - \hat{\theta}(n)\right) - \frac{A}{2}\sin\left(2\Omega_0 n + \theta(n) + \hat{\theta}(n)\right).$$

Since loop filter is a low pass filter the high frequency terms gets discarded leaving behind the low frequency term

$$= \frac{A}{2}\sin\left(\theta(n) - \hat{\theta}(n)\right)$$

Choosing appropriate loop constants is a very difficult step in Costas Loop design. The constants must be selected in such a way that the system should not be over damped or critically damped. Project involves realization of the loop functionality by writing matlab code with the help of appropriate loop constant values and various signal parameter values such as amplitude, frequency etc. of the message signal and the carrier signal. Overall loop performance is characterized by the phase error and the VCO output.

## III. FLOW OF THE PROJECT

A very first step of the project in Xilinx System Generator is to build a required DSB-SC AM system by using a predefined Xilinx block sets with the help of model based Matlab/Simulink environment. Designed algorithm is stored in the form of .MDL files. Every design must be invoked with System Generator Token which helps in generating a code automatically for the designed system in VHDL model. The System Generator design is synthesized with the help of Xilinx ISE tool which can be later implemented on FPGA with the help of Cross Core Embedded Studio and Chip Scope Pro Analyzer debugging tools.

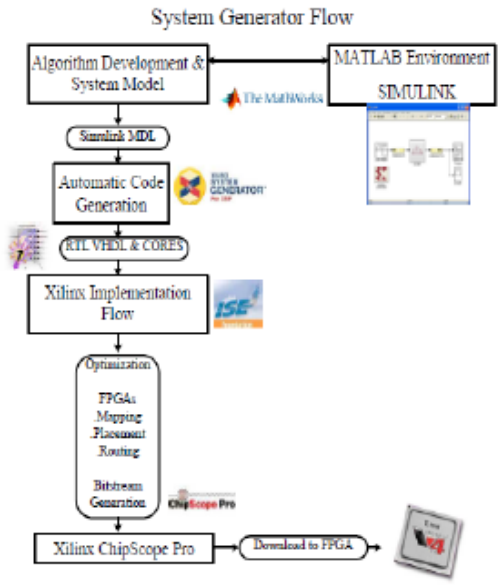


Fig3: system generator design flow

## IV. HARDWARE SYSTEM DESIGN

The hardware consists of two main sections, the Transmitter and the Receiver. Each section consists of a Digital Processor Module, ARTIX-7 FPGA, Trans Receiver AD9361, and a Digital Signal Processor (DSP).

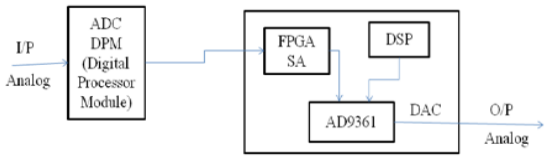


Fig4: Transmitter

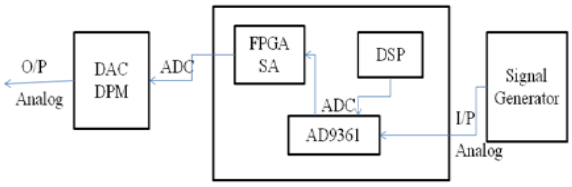


Fig5: Receiver.

## V. DESIGN AND SIMULATION RESULTS

Xilinx System Generator provides a group of Simulink blocks (models) for various hardware activities that could be implemented on numerous Xilinx FPGAs. These blocks can be used to design simulate the performance of the hardware system using Simulink environment. We can see that various predefined blocks and functions such as adder, multiplier, subtractor, DDS compiler, FDA tool, FIR compilers etc. are used to build the DSB_SC modulation and demodulation design.

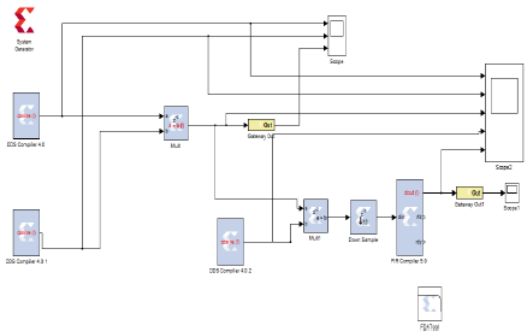

Fig6: DSB-SC Modulation & Demodulation block design.

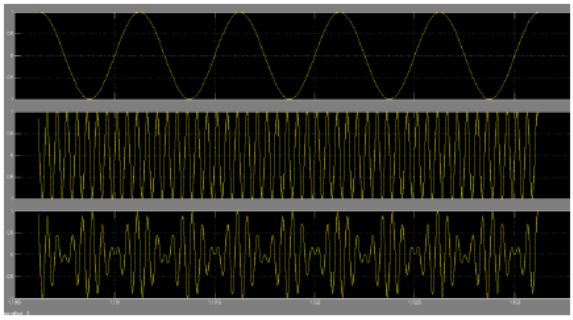

Fig7: Simulation result of DSB-SC Modulation.

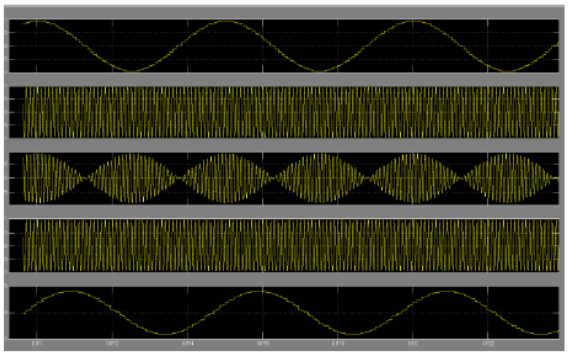

Fig8: Simulation result of DSB-SC Demodulation.

A Costas loop for the demodulation in receiver is designed as a subsystem unit which comprises further more subsystems exhibiting each and every functional blocks such as complex multiplier design, loop filter design etc.

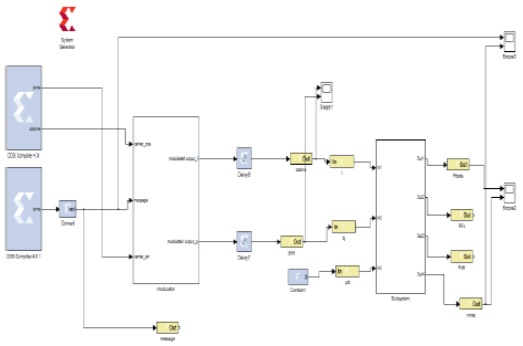

Fig9: Costas loop design for Carrier recovery & Demodulation.

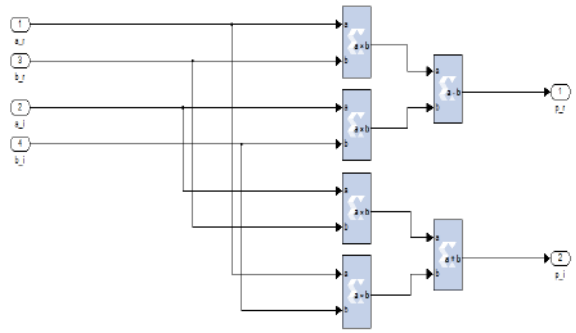

Fig10: Complex Multiplier design

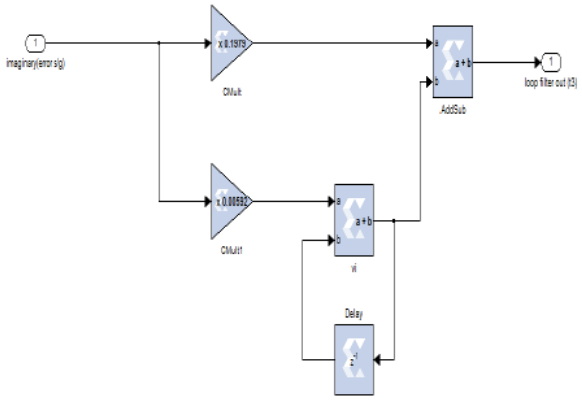

Fig11: Loop Filter design.

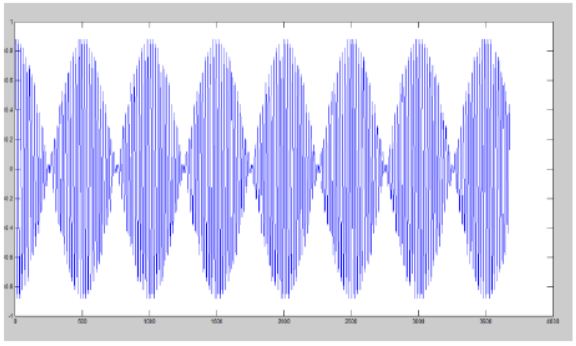

Fig12: Simulation result of modulated signal in a Costas Loop.

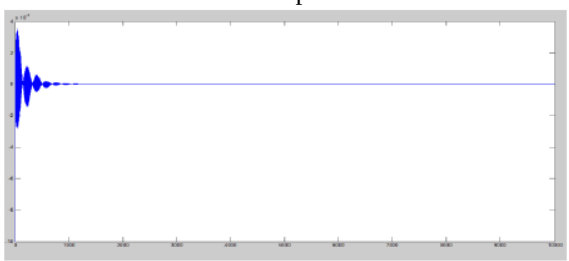

Fig13: Phase error in a Costas Loop.

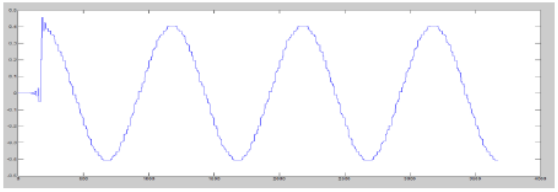

Fig14: Recovered message signal.

## VI. CONCLUSION

In this paper, a SDR with DSB-SC modulation technique has been prosperously designed using Xilinx tools. The PLL based Costas Loop and different coding scheme are implemented for carrier recovery and demodulation of the DSB-SC system. Software simulation and hardware implementation strategies display that this type of hardware/software design methodology is well appropriated to a broad range of applications in communication and signal processing.

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