QCA Based Design of Serial Adder

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Abstract - This paper presents the basics of quantum dot cellular automata along with the QCA logic devices such as the QCA wire, inverter and the majority gate. The four phases of the clocking have been discussed and also the implementation of the serial adder have been done using the QCA Designer tool. The 3 input serial adder is designed using a full adder, 2:1 decoder and a D flip-flop, each of which have been simulated separately and have been combined to form a serial adder. Simulation results follow in section 6 and conclusions are presented in section 7.

II. BACKGROUND

A. QCA basics

QCA technology is based on the interaction of bistable QCA cells constructed from four quantum dots. The cell is charged with two free electrons, which are able to tunnel between adjacent dots. These electrons tend to occupy antipodal sites as a result of their mutual electrostatic repulsion. Thus, there exist two equivalent energetically minimal arrangements of the two electrons in the QCA cell, as shown in Fig. 1. These two arrangements are denoted as cell polarization \( P = +1 \) and \( P = -1 \). By using cell polarization \( P = +1 \) to represent logic “1” and \( P = -1 \) to represent logic “0,” binary information is encoded in the charge configuration of the QCA cell [2][5].

![Fig. 1. QCA cell polarization.](image)

B. QCA logic devices

The fundamental QCA logic primitives include a QCA wire, QCA inverter, and QCA majority gate[4]-[6], as described below.

QCA Wire: In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells. The propagation in a 90° QCA wire is shown in Fig. 2. Other than the 90° QCA wire, a 45° QCA wire can also be used. In this case, the propagation of the binary signal alternates between the two polarizations [4].
**QCA Inverter:** The QCA cells can be used to form the primitive logic gates. The simplest structure is the inverter shown. Fig. 3, which is usually formed by placing the cells with only their corners touching. The electrostatic interaction is inverted, because the quantum-dots corresponding to different polarizations are misaligned between the cells [3].

**QCA Majority Gate:** The QCA majority gate performs a three-input logic function. A layout of a QCA majority gate is shown in Fig. 4.1. Assuming the inputs are a, b and c, the logic function of the majority gate is

\[ M(a, b, c) = ab + bc + ac. \]  

The tendency of the majority device cell to move to a ground state ensures that it takes on the polarization of the majority of its neighbours. The device cell will tend to follow the majority polarization because it represents the lowest energy state [3]. By fixing the polarization of one input to the QCA majority gate as logic “1” or logic “0” an AND gate or OR gate will be obtained, respectively, as shown in Fig. 4.2.

III. CLOCKING

The QCA circuits require a clock, not only to synchronize and control information flow but also to provide the power to run the circuit since there is no external source for powering cells. With the use of four phases clocking scheme in controlling cells, QCA processes and forwards information within cells in an arranged timing scheme. Cells can be grouped into zones so that the field influencing all the cells in the zones will be the same. A zone cycles through 4 phases. In the **Switch** phase, the tunneling barriers in a zone are raised. While this occurs, the electrons within the cell can be influenced by the Columbic charges of neighboring zones. Zones in the **Hold** phase have a high tunneling barrier and will not change state, but influence other adjacent. Lastly, the **Release** and **Relax** decrease the tunneling barrier so that the zone will not influence other zones. These zones can be of irregular shape, but their size must be within certain limits imposed by fabrication and dissipation concerns. Proper placement of these zones is critical to design efficiency. This clocking method makes the design of QCA different from CMOS circuits. [8].

The Fig. 5. Shows the four available clock signals. Each signal is phase shifted by 90’ degrees. When the clock signal is low the cells are latched. When the clock signal is high the cells are relaxed and have no polarization. In between the cells are either latching or relaxing when the clock is decreasing/increasing respectively.

![Fig. 5. Four phases of the clock.](image-url)
IV. QCA DESIGNER TOOL

QCA logic and circuit designers require a rapid and accurate simulation and design layout tool to determine the functionality of QCA circuits. QCADesigner gives the designer the ability to quickly lay out a QCA design by providing an extensive set of CAD tools. As well, several simulation engines facilitate rapid and accurate simulation. It is the first publicly available design and simulation tool for QCA. Developed at the ATIPS Laboratory, at the University of Calgary, QCADesigner currently supports three different simulation engines, and many of the CAD features required for complex circuit design. [9],[10].

V. QCA IMPLEMENTATION

A. Design of a Serial Adder

The serial adder is a combination of full adder, a 2:1 multiplexer and a D-flipflop. The design of the individual part is shown independently first and later on the combination of all the three will result in serial adder[11]. The schematic of the serial adder is shown in Fig.6.

![Fig.6 Schematic of a serial adder](image)

B. Design of a Full Adder

The schematic of a full adder is shown in Fig.7.1.

![Fig.7.1 Schematic of a full adder](image)

C. Layout for a 2:1 multiplexer

The multiplexer is controlled by Sel, which selects Cin during first bit addition and selects Co for the rest of the bits. While a multiplexer can be implemented using two transistors in CMOS technology, it requires three majority gates in QCA, and more importantly, it involves an extra clock cycle.

![Fig.7.3 Layout of a 2:1 multiplexer](image)

University of Notre Dame first proposed the design of a QCA full adder. The full adder is created from reduced majority logic. Reduction of sum of product logic to majority will almost always lead to smaller layouts [13].

The full adder is a good example of a system where the majority circuit uses less logic gates than the best sum of products decomposition [12].

The layout for a single full-adder is shown in Fig.7.2.

![Fig.7.2 Layout of a full adder](image)
multiplexer make it an expensive element in QCA designs. A multiplexer basically transmits one of the inputs to the output [11].

D. Layout for a D-flip flop

A serial adder implemented using CMOS technology needs a D flip-flop to buffer intermediate results. The silicon area of a D flip-flop is comparable to the silicon area of an FA. The D flip-flop is constructed from 68 cells. Using one of the D-flip-flops in a random-access memory and assuming standard dimensions for each cell results in memory capacities on the order of 5G-bits/cm² [13]. The layout of the D-flip-flop is shown in Fig.7.4.

The multiplexer is controlled by Sel, which selects Cin during first bit addition and selects CoL for the rest of the bits. While a multiplexer can be implemented using two transistors in CMOS technology, it requires three majority gates in QCA, and more importantly, it involves an extra clock cycle [13].

VI. SIMULATION RESULTS

For simulating the full adder followed by a serial adder coherence vector simulation method will be used since we are using different clock signals. Hence the parameters selected will be as follows:

- Dot diameter=5nm, Cell size=18nm,
- Temperature=1K, Relaxation time=1 e-15s, Time step=1 e-16s, Total simulation time=7 e-11s, Clock high=9.8e-22, Clock low=3.8 e-23, Clock amplitude factor=2, Radius of effect=80nm, Relative permittivity=12.9, Layer separation=11.5nm

Using the above parameters the simulation results for a full adder are as follows:

For a full adder circuit, the inputs selected are A=-1, B=1, and Cin. Thus the simulation outputs obtained are Sum=-1 and Cout=1. Thus, the circuit is verified with respect to the given inputs.

Using the above parameters the simulation results for a serial adder are as follows:

For a serial adder circuit, the inputs selected are A=-1, B=1, and Cin is selected with the help of a 2:1 multiplexer i.e. Cin is selected as 1 for the initial input. Thus, every time the carry propagated will be 1 and hence the simulation outputs obtained are Sum = -1 and Cout =1. Thus, the circuit is verified with respect to the given inputs.
For a serial adder circuit, the inputs selected are $A=-1$, $B=1$ and $C=1$ is selected with the help of a 2:1 multiplexer i.e. $Cin$ is selected as 1 for the initial input. Thus, every time the carry propagated will be 1 and hence the simulation outputs obtained are $Sum = -1$ and $Cout = 1$. Thus, the circuit is verified with respect to the given inputs.

VII. CONCLUSION

Using the QCA Designer tool the 3 input serial adder is designed using a full adder, 2:1 decoder and a D flipflop, each of which have been simulated separately and have been combined to form a serial adder. In this paper a single example is shown using the specific values, hence the complete truth table for the full adder and serial adder can be verified.

VIII. REFERENCES


