Low Power 8T SRAM Cell Design For
High Stability Video Applications

Maisagalla Gopal & Balwinder Raj
Department of ECE, National Institute of Technology Jalandhar, Punjab
E-mail : maisagallagopal.nitj@gmail.com, balwinderraj@gmail.com

Abstract – In this paper work has been carried out for a novel low power 8T Static Random Access Memory (SRAM) cell to enhance the stability and to save the SRAM power in real time video applications. For the validation of our proposed 8T SRAM cell, we compared our results with reported data. The size of the proposed cell is comparable to the existing 8T SRAM cell at same technology and design rules. In the proposed 8T SRAM cell, write operation done by charging / discharging single Bit Line (BL), which results in reduction of dynamic power consumption. The proposed 8T SRAM cell reduces the dynamic power 31.57% and leakage power 27.53%, comparing with the existing 8T SRAM cell. The existing 9T, 10T and higher transistor count, SRAM cells enhances the read stability with area and power penalty. In this paper stability has been also analyzed using N-curve metrics.

Index Terms- Dynamic power consumption, leakage power, stability, N-curve, Static Noise margin.

I. INTRODUCTION

As technology advances, more devices are integrated in a system and therefore a chip consumes more power [1]. Low power design is indispensable to realize battery operated systems. Due to the limited size of handheld devices, it is impossible to use larger batteries in it and short battery life time of a smaller battery limits the use of them [2]. Therefore low power design is essential to extend the battery life time. Most of the digital devices consists of memories and hence reducing power consumption of memories as well as area reduction is paramount important as of today to improve system performance, efficiency and reliability. One of the effective ways to reduce the leakage and dynamic power consumption is lowering the operating voltage due to its quadratic relationship [3], [4].

Static Random Access Memory (SRAM) is an indispensable part of most modern VLSI designs, because of its lower power consumption, high speed and it dominates silicon area in many applications [5], [6]. In scaled technologies maintaining high SRAM yield becomes more challenging since they are particularly vulnerable to process variations due to i) the minimum sized devices used in SRAM bit cells and ii) The large array sizes [7]. The amount of embedded SRAM in modern Systems on-Chips (SoC) increases to meet the performance requirements in each technology generation [8]. As the International Technology Roadmap for Semiconductors (ITRS) predicts, memory area is becoming 90% of the total chip area [9]. This trend is continuing also for real time video System on Chip (SoC). Two aspects are important for SRAM cell design: (i) the cell area and (ii) stability of cell. In today’s technology power dissipation in the memory circuits has become an important design consideration. As technology scaling, more devices are integrated into the system, as a result the corresponding leakage power increases. Lower voltages and smaller device dimensions cause a significant degradation of data stability in SRAM cell [10], which degrades the output video quality.

The remainder of this paper is organized as follows: section II describes the conventional 6T SRAM cell and its failures. Section III analyzes the 8T SRAM cell presented in [11]. In section IV, we describe the proposed 8T SRAM cell and analyze its effectiveness. Section V discusses the stability metrics. Section VI discusses the experimental conclusion between the cell presented in [11] & proposed cell, and finally in section VII we draw our conclusion, throughout this paper, we employ 180nm & 90nm technology for simulation.

II. CONVENTIONAL 6T SRAM CELL

Conventional 6T SRAM cell composed of two cross coupled inverters (M0, M1, M4 & M6) and two access transistors (M2 & M3). Gate terminals of the access transistors are connected to the Word Lines (WL), which is used to select the cell. Source/Drain terminals are connected to the Bit Lines (BL & BLB), which are used to perform the read and write operations on the cell [7].

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Conventional 6T SRAM cell exhibits poor stability during read operation, due to the voltage division between the access and driver transistors. With technology scaling, in the new coming manufacturing process the operating voltage and threshold voltage decrease and it demolishes the stability of the SRAM cell. Due to the direct paths between bit lines to the storage nodes, the data stored in conventional SRAM cell easily deteriorated by the external noise. Based on the above reasons conventional SRAM cell is not suitable for real time video applications [12].

The Static Noise Margin (SNM) of the conventional 6T SRAM cell can be enhanced by several times increasing the width of the driver transistor than the access transistor (standard method), which leads to enhancement in stability with area and leakage penalty.

III. 8T SRAM CELL

The 8T SRAM circuit described in this section [11]. The schematic of the 8T SRAM cell with transistors sized for a 90-nm CMOS technology shown in fig. 2. The primary source of instability problem in SRAM operation is disturbance of bit lines during read operation. The stability in 8T SRAM cell can be enhanced by isolating the read port from the write bit lines. The 8T SRAM cell composed of conventional 6T SRAM cell for writing operation and a transistor stack, which can be used for read operation. The read and write operations are controlled by separate signals Write Word Line (WWL) and Read Word Line (RWL).

During the read operation Read Bit Line (RBL) is pre charged to $V_{dd}$ and WWL is maintained at $V_{GND}$. Depends on the value stored in cross coupled inverters RBL, discharges (or) maintained at $V_{dd}$. If RBL discharges, it can be treated as the stored bit is ‘1’; otherwise it is ‘0’. The storage nodes are completely isolated from the write bit lines, which can increases the stability of the SRAM cell. During the write operation WBL and WBLB lines are pre charged to predetermined values. Then, asserting the write word line WWL and nodes attain the corresponding values from the bit lines. It uses the two additional Word Lines to perform read and write operations, when compared with 6T SRAM cell, which could increase the metal density, wire delay and dynamic power consumption [11], [13].

IV. PROPOSED 8T SRAM CELL

The schematic of proposed 8T SRAM cell, with transistors sized for 90nm is shown in fig. 3 to reduce the leakage current and dynamic power consumption.

The cell composed of write access transistor (M3), controlled by Write Word Line (WWL) and read access transistor (M8) is controlled by the Read Word Line (RWL). During the write operation WWL is transitions to high value and RWL and BLB both are maintained at $V_{GND}$. Hence, the read access transistor (M8) cut OFF. To write ‘1’ into the cell Bit Line (BL) is pre charged to a high value, then ‘1’ is forced through the write access
transistor (M3). Similarly, to write ‘0’ into the cell, BL is discharged. Hence, to perform write operation the proposed cell utilizing single BL, which could lead to reduction in the dynamic power consumption.

During read operation, RWL is transition to high value and WWL is maintained at $V_{\text{GND}}$. Hence the write access transistor is cut OFF. Prior to read operation BL and BLB are pre charged to $V_{\text{dd}}$. With this, storage nodes completely isolated from the Bit Lines (BL) during read operation, hence stability increases significantly. Assume that ‘1’ is stored left and ‘0’ is stored right side, then BL discharged through M7 and M8. Since, ‘M6’ is cut OFF there is no path to discharge the BLB. Hence BLB is held at high value. Alternatively, if ‘1’ is stored right side, BLB is discharged through ‘M6’ and ‘M8’. Since, ‘M7’ is cut OFF there is no path exists to discharge the BL. Hence, it can maintain at high value.

V. STATIC NOISE MARGIN ANALYSIS

Generally, the immunity of SRAM cell to static noise is expressed in terms of Static Noise Margin (SNM). It is defined as the maximum value of the DC noise voltage that can be tolerated by SRAM cell without altering the stored bits [9], [10]. Graphically, the SNM of 6T SRAM cell can be obtained by drawing the DC characteristics of a inverter and mirroring it. Then, finding the maximum possible square between them. This graphical method of finding SNM is called as “butterfly curve” [14]. As the technology scaling, cell becomes less stable with lower operating voltage, increasing leakage currents.

Cell becomes less stable during read operation as shown in fig. 4, because of the voltage dividing effect at the inverter which store ‘0’, will be pulled up. The drawback of the SNM metric using butterfly curve is that it does not contain automatic in-line testers. To measure the Static Current Noise Margin (SINM), still it requires mathematical manipulation from the measured data. Whereas, the N-curve contains the information of both read stability and write ability, thus it overcomes the limitations of SNM metric using butterfly curves [15].

N-CURVE METRICS ANALYSIS:

The N-curve gives the complete functional analysis of SRAM cell. A typical N-curve is shown in fig. 5 to describe the important parameters, which are useful to analyze the stability of the SRAM cell.

VI. RESULTS AND DISCUSSION

We have found the stability metrics using N-curve at different voltages for the conventional 6T SRAM cell and observed that at lower voltages the stability metrics has been reduced, which is shown in Table I.
Table-I: Stability Metrics using N-Curve

<table>
<thead>
<tr>
<th>$V_{dd}$ (V)</th>
<th>SVNM (mV)</th>
<th>SINM (uA)</th>
<th>WTV (mV)</th>
<th>WTI (uA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2</td>
<td>312.07</td>
<td>29.56</td>
<td>501.07</td>
<td>-12.29</td>
</tr>
<tr>
<td>1</td>
<td>290.91</td>
<td>25.08</td>
<td>472.48</td>
<td>-10.34</td>
</tr>
<tr>
<td>0.7</td>
<td>218.01</td>
<td>21.92</td>
<td>345.9</td>
<td>-4.853</td>
</tr>
<tr>
<td>0.5</td>
<td>175.90</td>
<td>10.25</td>
<td>243.43</td>
<td>-1.548</td>
</tr>
</tbody>
</table>

When observe the N-curve definitions for read stability and write ability of the SRAM cell, we can draw some conclusions with respect to the $V_{dd}$. By decreasing the $V_{dd}$ the read stability N-curve metrics degraded. Therefore, the stability of the cell is limited by the $V_{dd}$ scaling. The SINM can be enhanced for lower $V_{dd}$ by increasing the transistor widths, which of course, is at the expense of area. Fig. 6(a), 6(b) & 6(c) shows that an increase in $V_{dd}$ positively affects the read stability. To overcome the read destructive operation the value of the SVNM should as large as possible.

![Graph](a)

![Graph](b)

![Graph](c)

Fig 6: (a) SVNM and WTV metrics of the SRAM cell versus the supply voltage $V_{dd}$. (b) & (c) SINM and WTI metrics of the SRAM cell versus the supply voltage $V_{dd}$. All the N-curve metrics degrade with lower $V_{dd}$.

We have found the stability metrics using N-curve at two different voltages (1V & 1.2V) for the reference SRAM cell [11] and cell proposed in this paper. The proposed cell got the improved results, which is shown in Table II.
Table-II: Stability Metrics using N-Curve

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Reference cell at 1V</th>
<th>Proposed cell at 1V</th>
<th>Reference cell at 1.2V</th>
<th>Proposed cell at 1.2V</th>
</tr>
</thead>
<tbody>
<tr>
<td>SVN M (mV)</td>
<td>384.14</td>
<td>409.99</td>
<td>435.03</td>
<td>460.62</td>
</tr>
<tr>
<td>SINM (uA)</td>
<td>80.018</td>
<td>84.185</td>
<td>103.49</td>
<td>109.23</td>
</tr>
<tr>
<td>WTV (mV)</td>
<td>568.17</td>
<td>573.48</td>
<td>697.7</td>
<td>710.2</td>
</tr>
<tr>
<td>WTI (uA)</td>
<td>-29.40</td>
<td>-30.98</td>
<td>-36.63</td>
<td>-41.74</td>
</tr>
</tbody>
</table>

Fig. 7(a), 7(b), 7(c) & 7(d) shows the comparison between reference cell and proposed cell. Proposed achieved the improved results in terms of SVN M, SINM, WTV & WTI.

Figure 7: (a),(b),(c) & (d) are SVN M, SINM, WTV, WTI metrics of proposed and reference SRAM cells respectively versus power supply voltage $V_{dd}$.

DYNAMIC POWER AND LEAKAGE POWER ANALYSIS

As we explained earlier the dynamic power consumption will be increased by isolating the read port from the write bit lines. By reducing the switching activity and clock frequency, dynamic power can be lowered but it degrades the performance [16]. The proposed 8T SRAM cell reduces the dynamic power 31.57% and leakage power 27.53%.

Table III: comparison between reference cell and proposed cell for dynamic and leakage power

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Reference cell at 1V</th>
<th>Proposed cell at 1V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic power consumption</td>
<td>3.8uW</td>
<td>2.6uW</td>
</tr>
<tr>
<td>Leakage Current</td>
<td>4.83nA</td>
<td>3.5nA</td>
</tr>
</tbody>
</table>

VII. CONCLUSION

In this paper, we proposed a novel 8T SRAM cell to enhance the stability and to reduce the dynamic power consumption. The proposed cell is suitable for video applications in hand held devices. We compared & contrasted the results of our proposed 8T SRAM cell with reported data for the validation of our design approach. We analyzed stability metrics using N-curve, which gives the information about read stability and write ability. With this proposed 8T SRAM cell dynamic power and leakage power are reduced by 31.57% and 27.53% respectively.

VIII. REFERENCES

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