Generation of Radar Waveform Based on DDS Using FPGA And DAC

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Abstract : The generation of radar waveform is implemented and it is designed by using direct digital modulation method based on DDS. It is able to generate arbitrary signals whose frequency, amplitude and phases are controlled by the description words which will be given from external computer. By using Direct Digital Synthesis technique we can generate waveforms digitally and accurately. Direct Digital Synthesizer (DDS) [1] is a frequency synthesizer and it can generate arbitrary waveforms [2] by using single, fixed frequency reference clock. Some of the DDS Applications are: function generators, modulators. For implementing radar waveform generator along with DDS we need FPGA and DAC. To generate the waveform using DDS we need to store the discrete signal data in the internal RAM of FPGA. First in PC we need to program the information of the signal to be generated using MATLAB and ISE Design Tool. FPGA will be interfaced to the high speed DAC. Both FPGA and DAC will run under one reference clock. Finally the RADAR waveform generated will be of high spectral purity.

I. INTRODUCTION

The aim of this project is to design and implement a DDS architecture on a Field Programmable Gate Array (FPGA). Schematic and VHSIC hardware description language (VHDL) will be used to implement the proposed DDS architecture. The advantage of using an FPGA to implement the DDS is the speed but it also has other advantages. The FPGA behaves according to a “logic function”. The DDS architecture designed can be downloaded onto the FPGA as many times as wanted, there is no limit with different functionalities each time. If there is a mistake in the design, just fix the “logic function", re-compile, synthesize, build and re-download. Dedicated hardware would most likely require component changes. No PCB, solder or component to change. The designs can run much faster than if a board was to be designed with discrete components, since everything runs within the FPGA, on its silicon die. Then this FPGA will be interfaced with high speed DAC module which is implemented using IC-AD9736 [4]. The importance of this IC is that, it provides a better performance between the temperatures -60°C to 85°C. An advantage of AD9736 is it operates at high frequency and provides a sampling rate of 1200MSPS. After implementation of the DDS on an FPGA and DAC the performance of the output will be examined in Spectrum Analyzer which show the effect of non-ideal characteristics of building blocks of the DDS on the output spectrum.

II. DDS TECHNOLOGY

Direct digital synthesis (DDS) [1] is a method of producing an analog waveform usually a sine wave by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. Because operations within a DDS device are primarily digital, it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies. With advances in design and process technology, today’s DDS devices are very compact and draw little power.

Architecture of Direct Digital Synthesizer (DDS)

Here is a breakdown of the internal circuitry of a DDS device, its main components are a phase accumulator, a means of phase-to-amplitude conversion (often a sine look-up table), and a DAC. These blocks are represented in Figure 2.1.

![Fig 2.1 Components of a Direct Digital Synthesizer](image)

A DDS produces a sine wave at a given frequency. The frequency depends on two variables, the reference-clock frequency and the binary number programmed into the frequency register (tuning word).

The binary number in the frequency register provides the main input to the phase accumulator. If a sine look-up table is used, the phase accumulator computes a phase (angle) address for the look-up table, which outputs the digital value of amplitude—corresponding to the sine of that phase angle—to the DAC. The DAC, in turn, converts that number to a corresponding value of analog voltage or current. To generate a fixed-frequency sine wave, a constant value (the phase increment—which is determined by the binary number) is added to the phase accumulator with each clock cycle. If the phase increment is large, the phase accumulator will step...
quickly through the sine look-up table and thus generate a high frequency sine wave. If the phase increment is small, the phase accumulator will take many more steps, accordingly generating a slower waveform.

**Direct Digital Synthesizer Building blocks**

A DDS \(^{[1]}\) has both analog and digital blocks i.e. it is a mixed signal device. The digital blocks are the Phase Register, Phase Accumulator, and Phase-to-Amplitude Converter. While the analogue block are the Digital-to-Analogue Converter and Reconstruction Filter. The functionalities of each of these blocks of the DDS are discussed in this section.

**Phase Accumulator**

Continuous-time sinusoidal signals have a repetitive angular phase range of 0 to 2\(\pi\). The digital implementation is no different. The counter’s carry function allows the phase accumulator to act as a phase wheel in the DDS implementation.

To understand this basic function, visualize the sine-wave oscillation as a vector rotating around a phase circle (see Figure 2.2). Each designated point on the phase wheel corresponds to the equivalent point on a cycle of a sine wave. As the vector rotates around the wheel, visualize that the sine of the angle generates a corresponding output sine wave. One revolution of the vector around the phase wheel, at a constant speed, results in one complete cycle of the output sine wave. The phase accumulator (PA) provides the equally spaced angular values accompanying the vector’s linear rotation around the phase wheel. The contents of the phase accumulator correspond to the points on the cycle of the output sine wave. The phase accumulator is actually a modulo-M counter that increments its stored number each time it receives a clock pulse. The magnitude of the increment is determined by the binary-coded input word (M). This word forms the phase step size between reference-clock updates; it effectively sets how many points to skip around the phase wheel. The larger the jump size, the faster the phase accumulator overflows and completes its equivalent of a sine-wave cycle.

The number of discrete phase points contained in the wheel is determined by the resolution of the phase accumulator (n), which determines the tuning resolution of the DDS. For an n = 28-bit phase accumulator, an M value of 0000...0001 would result in the phase accumulator overflowing after 2\(^{28}\) reference-clock cycles (increments).

**Phase to Amplitude Converter**

A phase-to-amplitude lookup table is used to convert the PA’s instantaneous output value into the sine-wave amplitude information that is presented to DAC. In this project, the DDS’s RAM is a sine Look up Table (LUT). The accumulator output represents the phase of the wave as well as an address to a word, which is the corresponding amplitude of the phase in the LUT. This phase amplitude from the RAM LUT drives the DAC to provide an analog output. It is also called a digital Phase-to-Amplitude Converter (PAC), or polar-to-rectangular transformation (projection of the real or imaginary component in time), or (sine) waveform mapping device – a Memory. The lookup memory contains one cycle of the waveform to be generated. The size of the LUT is 2\(^n\) words. LUT translates truncated phase information, being in digital form, into quantized numerical waveform samples.
Digital to Analog Converter and Filter

The PA calculates a phase address for the look-up table, which outputs the digital value of amplitude corresponding to the sine of that phase angle to the DAC. The DAC, in turn converts that number to a corresponding value of analog voltage or current. The DDS system runs at the same reference clock for synchronization including the DAC. The DAC adds quantization errors at the output to the sine wave. Ideally, Sin(x)/x is used to filter the output of the DAC. It removes the extra frequency components added to the sine wave and hence produces a smooth sine wave.

A DAC is needed to transform the digital sine information into the analog domain. The DAC resolution determines the quality of the output waveform. Inherently, there will be distortion in the sine wave due to the discrete nature of the generation and conversion process. Typically the system is developed such that the error in the output waveform is dominated by the performance of the DAC.

The theoretical noise performance due to quantization error is given by

\[ 6.08 + m + 1.8 \text{dBc} \]

where \( m \) is the effective at-speed linearity of the DAC. DACs are usually specified for their DC linearity, but it is the AC characteristics that determine the noise performance. AC linearity is difficult measure, making it hard to predict actual noise performance of the DAC from data sheet parameters.

Additional degradation can be present in the output waveform related to both harmonics of the frequency being generated and the clock rate of the DAC. Non-ideal behaviour of the DAC will introduce distortion that shows up as harmonic spurs. Slow edge rates or delay mismatch on the signals switching the current or settling time, over/under shoot and glitch impulses at the DAC output can lead to this harmonic distortion. When operating well below Nyquist, these harmonics appear directly in the pass band and usually can be handled with appropriate filters at the output. However, when generating frequencies that approach Nyquist, these harmonics can mix with the reference clock and can produce spurs that fall back onto or near the fundamental. For high performance DDS, these are the factors that ultimately determine the quality of synthesized output.

Performance of DDS

A DDS has many advantages over its analog counterpart, the phase-locked loop (PLL), including much better frequency agility, improved phase noise, and precise control of the output phase across frequency switching transitions. Disadvantages include spurious due mainly to truncation effects in the NCO, crossing spurious resulting from high order (>1) Nyquist images, and a higher noise floor at large frequency offsets due mainly to the Digital-to-analog converter.

Because a DDS is a sampled system, in addition to the desired waveform at output frequency \( F_{\text{out}} \), Nyquist images are also generated (the primary image is at \( F_{\text{clk}} - F_{\text{out}} \) where \( F_{\text{clk}} \) is the reference clock frequency). In order to reject these undesired images, a DDS is generally used in conjunction with an analog reconstruction lowpass filter.

Phase noise and jitter

The superior close-in phase noise performance of a DDS stems from the fact that it is a feed-forward system. In a traditional phase locked loop (PLL), the frequency divider in the feedback path acts to multiply the phase noise of the reference oscillator and, within the PLL loop bandwidth, impresses this excess noise onto the VCO output. A DDS on the other hand, reduces the reference clock phase noise by the ratio \( f_{\text{clk}}/f_0 \) because its output is derived by fractional division of the clock. Reference clock jitter translates directly to the output, but this jitter is a smaller percentage of the output period (by the ratio above). Since the maximum output frequency is limited to \( f_{\text{clk}}/2 \), the output phase noise at close-in offsets is always at least 6dB below the reference clock phase-noise.

At offsets far removed from the carrier, the phase-noise floor of a DDS is determined by the power sum of the DAC quantization noise floor and the reference clock phase noise floor.

Spurious Free Dynamic Range

Spurious free dynamic range (SFDR) refers to the ratio (measured in decibels) between the highest level of the fundamental signal and the highest level of any spurious, signal including aliases and harmonically related frequency components in the spectrum. To obtain the very best SFDR, it is necessary to begin with a high-quality oscillator. SFDR is an important specification in an application where the frequency spectrum is being shared with other communication channels and applications. If a transmitter’s output sends spurious signals into other frequency bands, they can corrupt, or interrupt neighbouring signals.

The spectral purity of the DAC output is of primary concern in DDS application. A number of interacting factors complicate the prediction, measurement, and analysis of this performance. An ideal N-bit DAC produces harmonics in a DDS system. The amplitude of these harmonics is highly dependent upon the ratio of the output frequency to the clock frequency. The assumption that the quantization noise appears as white noise and is spread uniformly over the Nyquist bandwidth is not true in a DDS system. For instance, if


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the DAC output frequency is set to an exact sub multiple of the clock frequency, then the quantization noise is concentrated at multiples of the output frequency. If the output frequency is slightly offset, however, the quantization noise becomes more random, thereby giving an improvement in the effective SFDR. To obtain best SFDR clock and output frequencies must be carefully chosen.

In Analog to Digital Converter based systems, adding a small amount of random noise to the input tends to randomize the quantization errors and reduce this effect. The same thing can be done in a DDS system. A pseudo-random digital noise generator output can be added to the DDS sine amplitude word before being loaded into the DAC. In most DDS applications, however, there is enough flexibility in selecting the various frequency ratios so that dithering is not required.

### III. SYSTEM ARCHITECTURE

**A External Computer**

The external computer must consist of MATLAB and ISE Design Tool designed for Xilinx Vertex-6. The digital information of the signal is programed in MATLAB. In ISE, using VHDL description FPGA is configured to store data and clocking management inside FPGA. Details of the ports that are used in interfacing between FPGA and DAC are also entered.

**B FPGA**

The Virtex-6 FPGA ML605 Evaluation Kit provides a development environment for system designs that demand high-performance, serial connectivity and advanced memory interfacing. The ML605 is supported by pre-verified reference designs and industry-standard FPGA Mezzanine Connectors (FMC) which allow scaling and customization with daughter cards. Integrated tools help streamline the creation of elegant solutions to complex design requirements.

The important fundamental blocks of FPGA are IBUF, MMCM and OBUF.

IBUF converts differential clock pulses to single clock pulse.

MMCM is used for clock management it can provide number of clock pulses of different frequency.

OBUF converts single clock pulse to differential clock pulses.

**C DAC**

The AD9736, is a high performance, high frequency DAC that provide sample rates of up to 1200 MSPS, permitting multicarrier generation up to their Nyquist frequency. The AD9736 is a 14-bit DAC. It includes a serial peripheral interface (SPI) port that provides for programming of many internal parameters and enables readback of status registers. A reduced-specification LVDS interface is utilized to achieve the high sample rate. The output current can be programmed over a range of 8.66 mA to 31.66 mA. The AD9736 is manufactured on a 0.18 μm CMOS process and operates from 1.8 V and 3.3 V supplies for a total power consumption of 380 mW in bypass mode. It is supplied in a 160-lead chip scale ball grid array for reduced package parasitics.

**D CRO AND SPECTRUM ANALYSER**

CRO provides analog information of the waveform that is amplitude and frequency. Spectrum Analyzer provides the information about the non-linear characteristics and harmonics of the waveform.

### IV. IMPLEMENTATION DESIGN

The implementation of the entire system is carried out as shown in the figure 4.1.

**Fig 4.1 Block Diagram of Proposed System**

- The information of the signal is loaded into the FPGA RAM by using MATLAB and Simulink.
- This entire process is carried out in ISE Design Tool designed for Xilinx-Vertex-6.
• The data that is taken in by FPGA is buffered.

• For the synchronization purpose, management of the clock pulse inside the FPGA is done by MMCM.

• The simulation of the output data is verified in ISE design tool which is given in below figure 4.2.

![Fig 4.2 Simulation of FPGA Code](image)

- The interfacing of FPGA and DAC is done through FMC ports.
- The discrete sample values which are available in the RAM of FPGA is sent to High Speed DAC module.
- Since DAC operates at high frequency and better sampling rate, the data sent by the FPGA is converted to the analog signal with high precision.
- The output waveform is taken onto CRO for verification of frequency and amplitude.
- The non-ideal characteristics of output waveform and harmonics are analyzed in spectrum analyzer.

V. RESULTS

• The figure below gives the output waveform across CRO, where in the frequency and amplitude are verified.

![Fig 5.1 Sine wave output on CRO.](image)

• The figure below gives the output waveform across spectrum analyzer, the non-linear characteristics and harmonics are verified.

![Fig 5.2 Signal Frequency output spectrum.](image)

VI. CONCLUSION

In this paper, the radar waveform generator is designed using FPGA and DAC. This design shows the architecture of radar waveform generator which is designed using AD9736 DAC Module and FPGA.

REFERENCES


[2] Wenfeg Dong, Quan Liu, Shirui Peng and Haihong L “Design and Realization of Arbitrary Radar Waveform Generator based on DDS and


