Design and Synthesis of 8 Bit Reversible Arithmetic & Logical Unit ( ALU )

1Darshan H, 2Mohanraj R, 3Kavya H B, 4Monisha U K, 5Saroja Maralabhavi

Email: 1darshanramesh54@gmail.com, 2rmhnraj@gmail.com, 3kavya.charmi94@gmail.com, 4monishakantharaj77@gmail.com, 5saroja.marala@gmail.com

Abstract - Reversible computing has become most efficient technique to ensure reduced power dissipation in modern low power circuit design. Our paper presents the design of 8 bit reversible ALU which performs 7 arithmetic and 4 logical operations. The paper proposes 2 types of reversible ALU design. The ALU design-1 uses Peres Full Adder Gate (PFAG) and the ALU design-2 uses HNG gate as an adder circuit. Both the proposed designs are compared in terms of gate count, garbage output and quantum cost. The 2 ALU designs proposed are compared with a conventional 8 bit ALU in terms of power dissipation and propagation delay. The results show that the ALU design-2 is more efficient compared to proposed ALU design-1 and the conventional ALU.

Keywords: Low power VLSI, Reversible logic, gate count, quantum cost, power dissipation, propagation delay

I. INTRODUCTION

The performance of VLSI chips is practically limited by the large amount of heat released due to power dissipation. Less power dissipation is the core requirement of low power VLSI design. Reversible logic is capable of reducing the dissipation of power. Reversibility in computing ensures that no information at different states of computation is lost. Reversible computing finds a wide range of applications in low power CMOS and Optical information processing, DNA computing, cryptography, quantum computation and nanotechnology.

In irreversible logic circuits, the power is dissipated in the form of heat due to the loss of information. For every bit of information lost, kTln2 joules of energy is dissipated (where ‘k’ is the Boltzmann’s constant and ‘T’ is the operating temperature). This power dissipation seems to be very small at room temperature; but as the number of lost bits increase, more heat is dissipated which has a negative impact on performance of the circuit and also the lifespan of circuit components.

A research on this issue led to an analysis which gives a solution to this problem. It was shown that as long as the system can reproduce the inputs from their outputs, the power dissipation would not occur. The reversible computations can generate inputs from outputs and the computation history is stored. In reversible logic circuits, each input vector has a unique output vector and there is one-to-one mapping between the input and output assignments.

An Arithmetic and Logical Unit (ALU) is a multipurpose circuit which performs several possible operations on the two input operands. The ALU needs to operate continually throughout the lifetime of the processor. Hence it is to be seen that the performance of ALU is superior and the circuit elements are prevented from being damaged due to heat dissipation. This can be done by designing a reversible ALU.

The paper proposes 2 designs of 8 bit reversible ALU which uses two different reversible adder circuits. The proposed ALU design-1 & design-2 performs 7 arithmetic and 4 logical operations. The ALU design-1 uses Peres Full Adder Gate (PFAG) and the ALU design-2 uses HNG gate as an adder circuit. Both the proposed designs are compared in terms of gate count, garbage output and quantum cost. The 2 ALU designs proposed are compared with a conventional 8 bit ALU in terms of power dissipation and propagation delay.

A brief overview of the reversible gates used for our design is presented in section II. Section III describes the 2 proposed ALU designs. The simulation results and comparison of reversible and conventional 8 bit ALU is presented in section IV. The conclusion along with future scope is discussed in section V.

II. BASIC REVERSIBLE GATES

A reversible gate in an n x n logic circuit and there is always one-to-one mapping between the inputs and outputs. This ensures that inputs can be uniquely recovered from the outputs. The parameters that decide the performance of a reversible circuit are:

1. Gate Count: Number of gates used to completely design a reversible circuit. Gate count should always be minimum.

2. Constant Inputs: The inputs that should be maintained either at ‘0’ or ‘1’ in order to synthesize the given logical function. The number of constant inputs should be minimum.

3. Garbage outputs: The number of unused outputs present in the reversible logic circuit. The number of garbage outputs must be minimum.

4. Quantum Cost: The cost of circuit in terms of the cost of a primitive gate. Quantum cost for any reversible gate must be minimum.

In the proposed ALU designs, feynmann, fredkin, RI, peres and HNG gates are used and these gates are described below.

Feynman Gate: It is also known as controlled not (CNOT) gate. It is a 2x2 reversible gate with quantum cost=1. This gate is useful or duplication of required
outputs. Figure 1 shows the inputs and outputs of Feynman gate.

Fredkin Gate: It is a 3x3 reversible gate with a quantum cost of 5. Figure 2 shows the quantum operation of FG.

RI Gate: It is 3x3 reversible gate shown in Figure 3 which require only 7 transistors for transistor level implementation. RI gate is made of 1 xor, 1 or, 1 not and 3 and gates.

Peres Gate: It is also a 3x3 reversible gate with quantum cost 4. It is made from 2 xor gates and 1 and gate. The quantum operation of peres gate is depicted in Figure 4.

III. PROPOSED ALU DESIGN

The proposed reversible 8 bit ALU is designed so that it performs similar to that of a conventional 8 bit ALU. The proposed system uses 5 constant inputs: C1='1'; C2='1'; C3='0'; C4='0'; C5='0'. The reversible ALU consists of three main logic circuits namely (i) Control unit (ii) Reversible adder (iii) Multiplexer

Figure 5 indicates the general block diagram of the reversible ALU proposed in this paper.

1. Control Unit:
Control unit in reversible ALU performs the arithmetic operations in the ALU. The proposed control unit comprises of three feynmann gates, three RI gates and one fredkin gates. The control unit has four constant input signals and eight garbage outputs in the 2 reversible ALU designs proposed as depicted in Figure 6. The four control signals (s2, s1, s0, cin) monitors the operations to be performed on two input operands.

2. Reversible Adder:
The reversible adder circuit used in the proposed designs 1 & 2 uses one constant input and has 2 garbage outputs. The 3rd and 4th outputs are taken as a function of Sum & Cout respectively. The outputs of reversible full adder are given by the equations below.

\[ \text{Sum} = A \oplus B \oplus C_{in} \]
\[ \text{Carry} = (A \oplus B) \& C_{in} \oplus (A \& B) \]

(a) PFAG (Peres Full Adder Gate):
The PFAG gate is 4x4 reversible full adder gate that comprises of 2 Peres gates as shown in Figure 7. The Quantum cost of PFAG gate is 8.
(b) HNG Gate:

HNG gate is a 4x4 reversible gate with a quantum cost equal to 6.

3. Multiplexer:

The reversible 2x1 multiplexer is implemented using a 3x3 fredkin gate as shown in Figure 8. Two reversible multiplexers are used; one used to select either F or Cout at the output, the other one to select either arithmetic or logical output. The select lines used for mux1 and mux2 are s1^s0 and s2 respectively.

4. Proposed ALU Design-1

Figure 9 depicts the proposed reversible 8-bit ALU design-1.

5. Proposed ALU Design-2

Figure 10 shows the block diagram of proposed reversible 8 bit ALU design-2.

IV. RESULTS

Table 1 and Table 2 show the performance comparison of the conventional ALU design with the proposed reversible ALU designs. For comparison, number of gate count, garbage output, quantum cost, and propagation delay are considered as the performance matrices.

<table>
<thead>
<tr>
<th>Parameter which has to be compared</th>
<th>Gate count</th>
<th>Garbage output</th>
<th>Quantum cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design 1: Control Unit + PFAG</td>
<td>9</td>
<td>10</td>
<td>28</td>
</tr>
<tr>
<td>Design 2: Control Unit + HNG</td>
<td>8</td>
<td>10</td>
<td>26</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Number of Bits</th>
<th>Reversible ALU Design 1 (ns)</th>
<th>Reversible ALU Design 2 (ns)</th>
<th>Conventional ALU (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-bit</td>
<td>7.75</td>
<td>7.17</td>
<td>8.17</td>
</tr>
<tr>
<td>4-bit</td>
<td>8.38</td>
<td>8.13</td>
<td>8.73</td>
</tr>
<tr>
<td>8-bit</td>
<td>8.79</td>
<td>8.29</td>
<td>9.43</td>
</tr>
<tr>
<td>16-bit</td>
<td>7.39</td>
<td>8.26</td>
<td>9.13</td>
</tr>
</tbody>
</table>

V. CONCLUSION

In this paper, the reversible ALU design is proposed with two unique design paradigms. The proposed reversible ALU designs are verified using Xilinx tool. Both proposed designs are analyzed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The simulation results illustrate that the proposed reversible ALU design-2 outperforms the proposed reversible ALU design-1 and conventional ALU design.

REFERENCES


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